DS33Z44DK
Ethernet Transport Design Kit

www.maxim-ic.com

GENERAL DESCRIPTION

The DS33Z44 design kit is an easy-to-use evaluation board for the DS33Z44 Ethernet transport-over-serial link device. The DS33Z44DK is intended to be used with a resource card for the serial link. The serial link resource cards are complete with transceivers, transformers, and network connections. Dallas' ChipView software is provided with the design kit, giving point-and-click access to configuration and status registers from a Windows®-based PC. On-board LEDs indicate receive loss-of-signal, queue overflow, Ethernet link, Tx/Rx, and interrupt status.

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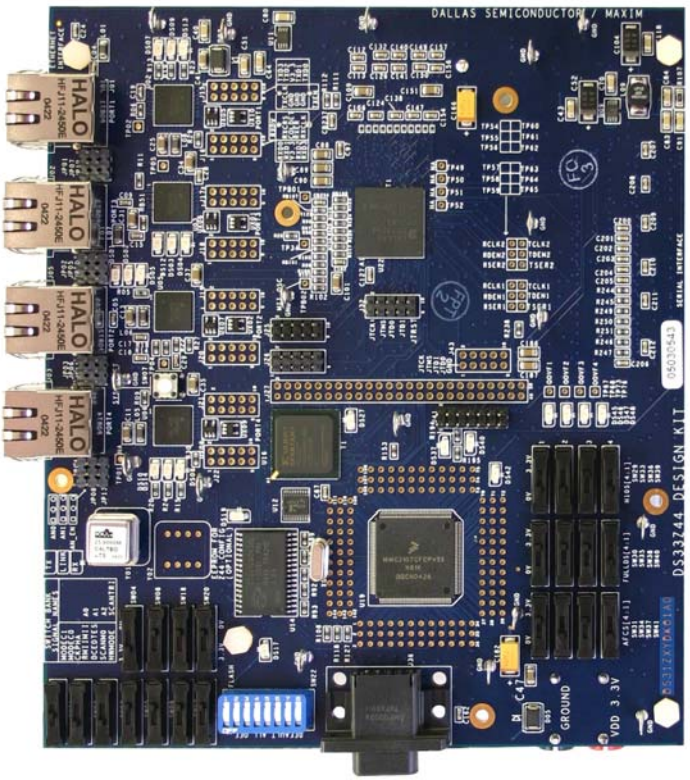
ORDERING INFORMATION

PART	DESCRIPTION
DS33Z44DK	DS33Z44 demo card, T3/E3, T1/E1 transceiver resource card included

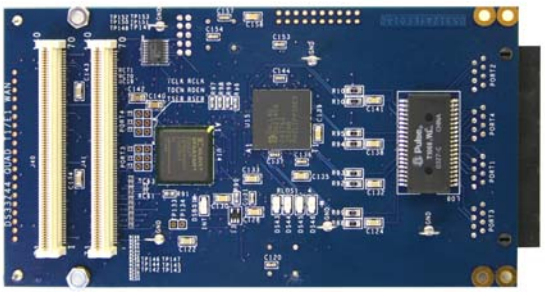


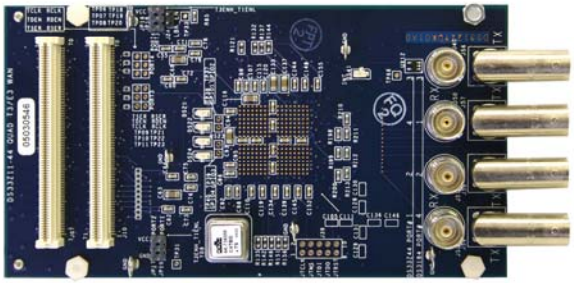
FEATURES

- **Demonstrates Key Functions of DS33Z44 Ethernet Transport Chipset**
- **Includes Two Resource Cards: One with DS21458 T1/E1 SCT and one with DS3174 T3/E3 SCT, Transformers, BNC and RJ48 Network Connectors, and Termination**
- **Provides Support for Hardware and Software Modes**
- **On-Board MMC2107 Processor and ChipView Software Provide Point-and-Click Access to the DS33Z44 Register Set**
- **All DS33Z44 Interface Pins are Easily Accessible for External Data Source/Sink**
- **LEDs for Loss-of-Signal, Queue Overflow, Ethernet Link, Tx/Rx, and Interrupt Status**
- **Easy-to-Read Silkscreen Labels Identify the Signals Associated with All Connectors, Jumpers, and LEDs**

DESIGN KIT CONTENTS

- DS33Z44DK Main Board
- Quad-Port Serial Card with DS21458 T1/E1 SCT
- Quad-Port Serial Card with DS3174 T3/E3 SCT
- CD_ROM
  - o ChipView Software and Manual
  - o DS33Z44DK Data Sheet
  - o Configuration Files





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COMPONENT LIST

Table 1 shows the component list for the DS33Z44 and DS33Z11/DS33Z41 design kits and resource cards. This BOM contains the part listing for five boards. These boards are the DS33Z11DK, DS33Z44DK, DS21458RC, DS3174RC, and DS2155-DS21348-DS3170RC. Each reference designator is only used once. For example, U18 only appears on the DS33Z11DK and is not used on any of the other boards. See Table 2.

Table 1. Component List (Decoupling Caps Not Shown)

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
U18	1	ELITE 10/100 ETHERNET TRANSPORT OVER SERIAL LINK 14X14 CSBGA 169 PIN	Dallas Semiconductor	DS33Z11
U20	1	3.3V T1.E1.J1 QUAD TRANSCEIVER 0-70C 256P BGA	Dallas Semiconductor	DS21458
U22	1	QUAD 10/100 ETHERNET EXTENSION TO WAN 17X17 PBGA 256 PIN	Dallas Semiconductor	DS33Z44
U23	1	DS3/E3 SCT, 11X11 CSBGA, 100 PIN	Dallas Semiconductor	DS3170
U24	1	T1/E1/J1 XCVR 100P QFP 0-70C	Dallas Semiconductor	DS2156L
U25	1	3.3V LIU	Dallas Semiconductor	DS21348
UB08	1	QUAD TRIPLE DUAL SINGLE ATM PACKET PHYS FOR DS3 E3 STS1 0-70C 400P BGA	Dallas Semiconductor	DS3184
U01, U09	2	SOIC 8PIN STEP-UP DC-DC CONVERTER 0.5A LIMIT	Maxim	MAX1675EUA
U07, U11	2	8-Pin µMAX/SOIC 1.8V or Adj	Maxim	MAX1792EUA18
U13, UB01	2	MICROPROCESSOR VOLTAGE MONITOR, 2.93V RESET, 4PIN SOT143	Maxim	MAX811SEUS-T
U21, UB07	2	Dual RS-232 transceivers with 3.3V/5V internal capacitors	MAXIM	NA
U31, UB06, UB11	3	8-Pin µMAX/SOIC 2.5V or Adj	Maxim	MAX1792EUA25
C11, C13, C16, C25, C27, C31–C35, C37, C41, C47, CB10, CB63, CB114, CB128, CB164, CB496	19	1206 CERAM 10uF 10V 20%	Panasonic	ECJ-3YB1A106M
CB390, CB391, CB395, CB396	4	1206 CERAM 0.1uF 25V 10%	Panasonic	ECJ-3VB1E104K
D01–D03, D05, DB03–DB05	7	SCHOTTKY DIODE, 1 AMP 40 VOLT	International Rectifier	10BQ040
DS01, DS07, DS10–DS12, DS17, DS20	7	LED, AMBER, SMD	Panasonic	LN1451C
DS02, DS03, DS09, DS14, DS15	5	L_LED, GREEN, SMD	Panasonic	LN1351C
DS04–DS06, DS08, DS13, DS16, DS18, DS27, DS28, DS35, DS37, DS38, DS40	13	LED, RED, SMD	Panasonic	LN1251C
DS19, DS43	2	LED, GREEN, SMD	Panasonic	LN1351C
DS21–DS26, DS30, DS32–DS34, DS36, DS39, DS41, DS42, DS44–DS48	19	L_LED, RED, SMD	Panasonic	LN1251C
GND_TP01–GND_TP07, GND_TP09—GND_TP44, GND_TP46–GND_TP68, GND_TPB01–GND_TPB10	76	STANDARD GROUND CLIP	KEYSTONE	4954
H1–H8, H17–H19	8	KIT, 4-40 HARDWARE, .50 NYLON STANDOFF AND NYLON HEX-NUT	NA	Lab Stock

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
H9–H16	16	KIT, 4-40 HARDWARE, 1.12 NYLON STANDOFF AND NYLON HEX-NUT (1.12 STANDOFF PN = 4807K-ND)	NA	Lab Stock
J01–J05	5	CONNECTOR, FASTJACK SINGLE, 8 PIN	Halo Electronics	HFJ11-2450E
J06, J41	2	100 MIL 2*7 POS JUMPER	NA	Lab Stock
J07–J12	6	RECEPTACLE, SMD, 140 PIN, .8MM, 2 ROW VERTICAL	AMP	5-179010-6
J13–J22	10	L_TERMINAL STRIP, 10 PIN, DUAL ROW, VERT DO NOT POPLUATE	NA	Lab Stock
J23, J29, J32, J38, J39, J43, J44, J47, JB07	9	L_TERMINAL STRIP, SHROUDED, 10 PIN, DUAL ROW, VERT	3M Electronics	2510-6002UB
J24, J30, J31, J33	4	100 MIL 2 POS JUMPER	NA	Lab Stock
J25, J26, J45, J46	4	TERMINAL STRIP, 10 PIN, DUAL ROW, VERT	NA	Lab Stock
J27, J42	2	CONN 50 PIN, 2 ROW, POSTS VERT, MOTHERBOARD FOOTPRINT	SAMTEC	TSW-125-07-T-D
J28, J36	2	L_CONN, DB9 RA, LONG CASE	AMP	747459-1
J48, J54, JB01	3	SOCKET, BANANA PLUG, HORIZONTAL, BLACK	Mouser Electronics	164-6218
J49–J52	4	CONNECTOR BNC 75 OHM VERTICAL 5PIN	Cambridge	CP-BNCPC-004
J53, JB02, JB08	3	SOCKET, BANANA PLUG, HORIZONTAL, RED	Mouser Electronics	164-6219
J55, JB11	2	L_RJ48 8 PIN SINGLE PORT CONNECTOR	MOLEX	15-43-8588
J56–J59, J61, J63	6	CONNECTOR BNC 75 OHM RA 5PIN	Trompetor	UCBJR220
J60, J62, J64, J65	4	CONNECTOR BNC RA 5PIN	Trompetor	UCBJR220
JB05, JB06, JB09, JB10, JB13, JB14	6	PLUG, SMD, 140 PIN, .8MM, 2 ROW VERTICAL	AMP	179031-6
JB12	1	RA RJ45 8PIN 4PORT JACK	MOL	43223-8140
JP01–JP19	19	100 MIL 3 POS JUMPER	NA	NA
L01, L03–L08, LB01, LB02	9	FERRITE 3A 100 OHM AT 100 MHZ 1206 SMD	Steward	HI1206N101R-00
L02, L09	2	INDUCTOR 22.0uH 2PIN SMT 20%	Coiltronics	UP1B-220
L10	1	XFMR 1-2CT XMIT, 1-1CT RCV, 40P WIDE SOIC	Pulse	T1068
R01, R02, RB10, RB11, RB18, RB19, RB22, RB23, RB26, RB27	10	RES 0603 54.9 Ohm 1/16W 1%	Panasonic	ERJ-3EKF54R9V
R03, R04, RB12, RB13, RB20, RB21, RB24, RB25, RB28, RB29	10	RES 0603 49.9 Ohm 1/16W 1%	Panasonic	ERJ-3EKF49R9V
R05, R06, R08, R09, R11	5	RES 0603 10.0K Ohm 1/16W 1% - Must be 1% tolerance	Panasonic	ERJ-3EKF1002V
R07, R12, R16, R79, R160, R244, R248, R250, R251, R254, R255, RB126, RB143, RB147, RB150, RB157	16	RES 0603 1.0K Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ102V
R10, R107	2	RES 1206 5.6 Ohm 1/8W 5%	Panasonic	ERJ-8GEYJ5R6V
R132, R137, R142, R144, R156, RB194, RB208, RB227	8	L_RES 0603 0 Ohm 1/16W 1%	AVX	CJ10-000F

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
R13–R15, R18–R20, R22, R23, R29, R30, RB01, RB03, RB07, RB09, RB15–RB17, RB30–RB32, RB34–RB38, RB41, RB44, RB47, RB48, RB50–RB52, B55, RB60, RB62, RB72, RB73, RB75, RB80, RB82	40	RES 0603 5.1K Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ512V
R17, R21, R25–R28, R31, R55, R57–R59, R71, R74–R76, R83, R96–R102, R105, R106, R109, R111, R112, R115–R117, R120, R122–R126, R128, R133, R134, R140, R141, RB61, RB96, RB97, RB99, RB100, RB102–RB110, RB112, RB114–RB119, RB121, RB123–RB125, RB127, RB128, RB130, RB131, RB133, RB135–RB138, RB145, RB148, RB149, RB160, RB161, RB164, RB165, RB167–RB171, RB173–RB181, RB184, RB187, RB311, RB320, RB335, RB339, RB359	104	RES 0603 30 Ohm 1/16W	Panasonic	ERJ-3GEYJ300V
R171, R172, R174, R175, R190, R191, R240, R241	8	L_RES 0805 0.0 Ohm 1/10W 5%	Panasonic	ERJ-6GEY0R00V
R198–R200, R210–R213, RB306, RB325, RB326	10	RES 0603 332 Ohm 1/16W 1%	Panasonic	ERJ-3EKF3320V
R201–R208, RB321–RB324, RB327–RB330	16	RES 1206 0 Ohm 1/8W 5%	Panasonic	ERJ-8GEYJ0R00V
R239, RB349	2	RES 0805 51.1 Ohm 1/10W 1%	Panasonic	ERJ-6ENF51R1V
R24, R114, R197, RB14, RB33, RB40, RB42, RB43, RB49, RB53, RB54, RB57–RB59, RB71, RB77, RB78, RB152–RB156, RB221, RB234, RB251, RB284, RB304, RB331, RB332, RB342, RB344, RB350, RB354, RB360	34	L_RES 0603 330 Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ331V
R242, R243, RB144, RB166, RB355–RB358, RB368–RB371	12	RES 0603 51 Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ510V
R32, R70, R78, R161, R176, R194, R195, R237, R238, RB129, RB134, RB146, RB193	13	RES 0603 330 Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ331V
R33–R54, R60–R69, R72, R73, R131, R136, R143, R147, R150, R154, R158, R163, R166, R169, R173, R178–R189, R215–R228, RB89–RB95, RB101, RB188–RB191, RB196–RB199, RB202–RB205, RB210–RB213, RB216–RB219, RB223–RB226, RB230–RB233, RB239–RB242, RB244–RB249, RB252–RB260, RB265–RB268, RB270-RB282, RB289–RB297	152	RES 0402 30 Ohm 1/16W 5%	Panasonic	ERJ-2GEJ300X
R56, R90	2	RES 0603 1.0M Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ105V
R77, RB159	2	L_RES 1206 0 Ohm 1/8W 5%	Panasonic	ERJ-8GEYJ0R00V
R80, R81, R84, R87, R89, R91–R93, R95, R108, R110, R118, R127, R152, R153, R196, R209, R214, R229–R236, RB200, RB237, RB238, RB263, RB264, RB286, RB287, RB300, RB301, RB333, RB364	37	RES 0603 10K Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ103V

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
R85, R88, R94, R104, R113, RB02, RB04–RB06, RB08, RB39, RB45, RB46, RB56, RB63–RB70, RB76, RB83, RB98, RB183, RB185, RB192, RB209, RB228, RB302, RB303, RB305, RB338, RB340, RB341, RB346–RB348, RB351–RB353, RB361–RB363, RB365–RB367	48	RES 0603 2.0K Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ202V
R86, R103, R119, R121, R129, R130, R135, R138, R139, R145, R146, R149, R151, R157, R162, R164, R167, R168, R170, R177, R192, R193, R245-R247, R249, R252, R253, R256, R257, RB74, RB79, RB132, RB139-RB141, RB151, RB162, RB163, RB172, RB182, RB186, RB206, RB207, RB214, RB215, RB220, RB222, RB229, RB235, RB236, RB243, RB250, RB261, RB262, RB269, RB308–RB310, RB343, RB345	61	L_RES 0603 10K Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ103V
RB201, RB285	2	RES 0805 330 Ohm 1/10W 5%	Panasonic	ERJ-6GEYJ331V
RB283	1	RES 0603 10K Ohm 1/10W 5% - SEE SPECIAL INSTRUCTIONS	Panasonic	603_ERJ-3GEYJ103V
RB298, RB299, RB312–RB319, RB336, RB337	12	RES 0805 61.9 Ohm 1/10W 1%	Panasonic	ERJ-6ENF61R9V
RB81, RB84–RB88, RB111, RB113, RB120, RB122	10	RES 0603 DO NOT POPULATE	NA	NA
SW01–SW05, SW08–SW21, SW24–SW26, SW29–SW31, SW33–SW44	37	L_SWITCH, SP3T SLIDE, 4PIN TH	Tyco	3-1437575-3
SW06, SW22	2	L_SWITH 8POS 16PIN DIP LOW PROFILE	AMP	435668-7
SW07, SW23	2	SWITCH MOM 4PIN SINGLE POLE	Panasonic	EVQPAE04M
SW27, SW28, SW32	3	L_DIPSWITCH, 10 POS	AMP	435668-9
T01, T03	2	XFMR 16P SMT	Pulse	TX1099
T02, TB01	2	XFMR, OCTAL T3/E3, 1 TO 2, SMT 32 PIN	Pulse	T3049
TP01–TP78, TPB01, TPB02	80	TESTPOINT, 1 PLATED HOLE, DO NOT STUFF	NA	NA
U02–U06	5	IC, DsPHYTER11-SINGLE 10/100 ETHERNET TRANSCEIVER, 65 PIN LLP	National Semiconductor	DP83847ALQA56A
U08, U12, U29	3	1MBit Flash based config mem	Avnet	XCF01SV020C
U10	1	XILINX SPARTAN xc200 2.5V FPGA,256 PIN BGA	Xilinx	XC2S200-5FG256C
U14, U26, U30, UB05	4	CYPRESS SRAM, LAB STOCK	NA	NA
U15, U19	2	mmc2107 processor	Motorola	MMC2107
U16, U27	2	XILINX SPARTAN 2.5V FPGA,256 PIN BGA	Xilinx	XC2S50-5FG256C
U17, U28, U32	3	10 pin res pack, 10K ohm	NA	NA
UB02, UB03, UB04	3	100 PIN CPLD	XILINX	XC95144XL-10TQ100C
UB09, UB10	2	SYNCHRONOUS DRAM, 1MEGX32X4 BANKS, TSOP 86 PIN	Micron	MT48LC4M32B2TG-7

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
UX01–UX12, UXB02–UXB04, UXB06–UXB08	18	HIGH SPEED BUFFER	Fairchild	NC7SZ86
UXB01, UXB05	2	HIGH SPEED INVERTER	Fairchild	NC7SZ86
X01, X02	2	XTAL LOW PROFILE 8.0MHZ	ECL	EC1-8.000M
Y01, Y09	2	OSCILLATOR, CRYSTAL CLOCK, 3.3V - 25.000 MHZ, Low Jitter required for PHY	SaRonix	NTH089AA3-25.000
Y02, Y13	2	SPI SERIAL EEPROM 16K 8 PIN DIP 2.7V NEEDS SOCKET	Atmel	AT25160A-10PI-2.7
Y03	1	OSCILLATOR, CRYSTAL CLOCK, 3.3V - 2.048 MHZ	SaRonix	NTH039A3-2.0480
Y05, Y06	2	OSCILLATOR, CRYSTAL CLOCK, 3.3V - 100.000 MHZ	SaRonix	NTH089A3-100.0000
Y07	1	OSCILLATOR, CRYSTAL CLOCK, 3.3V - 44.736 MHZ	SaRonix	NTH089AA3-44.736
Y08	1	OSCILLATOR, CRYSTAL CLOCK, 5.0V - 44.736 MHZ	SaRonix	NTH089AA-44.736
YB02	1	L_OSCILLATOR, CRYSTAL CLOCK, 3.3V - 2.048 MHZ	SaRonix	NTH039A3-2.0480

Figure 1. System Floorplan

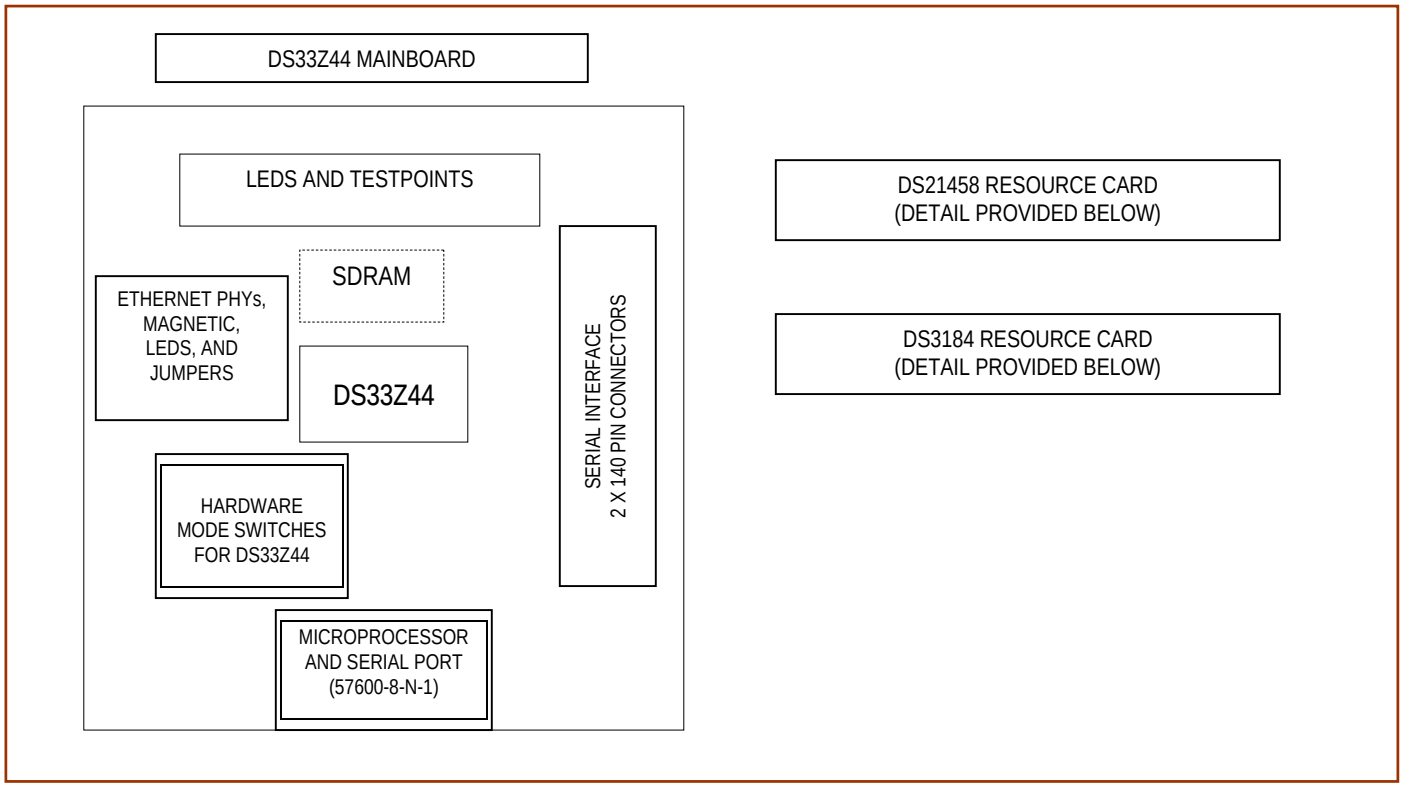
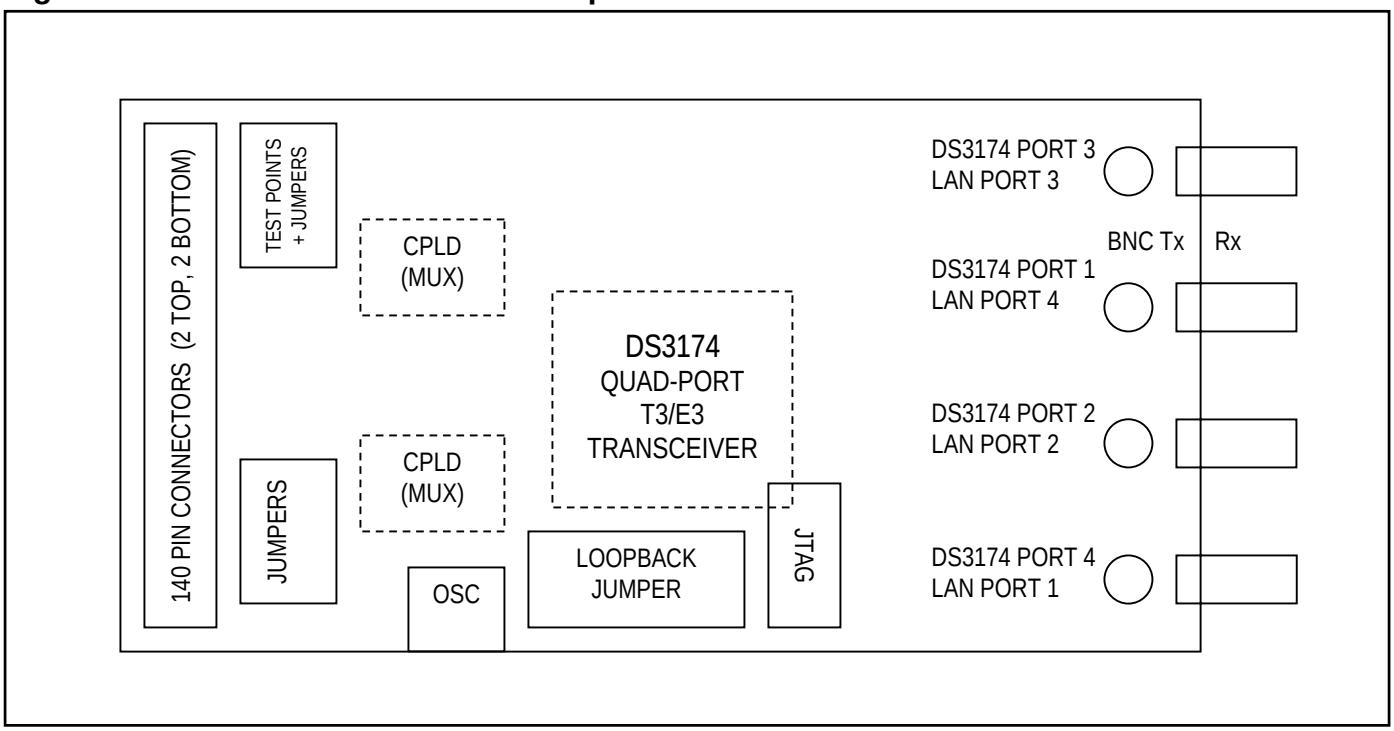


Figure 2. DS3174 Resource Card Floorplan



The DS3174 quad T3/E3 PC board floorplan is shown in Figure 2. Jumpers JP16, JP17, JP18, and JP19 are 3-pin jumpers used to tri-state/enable T3/E3 ports. With the board oriented as shown in Figure 2, the top 2 pins of each jumper would be connected to enable T3/E3 traffic.

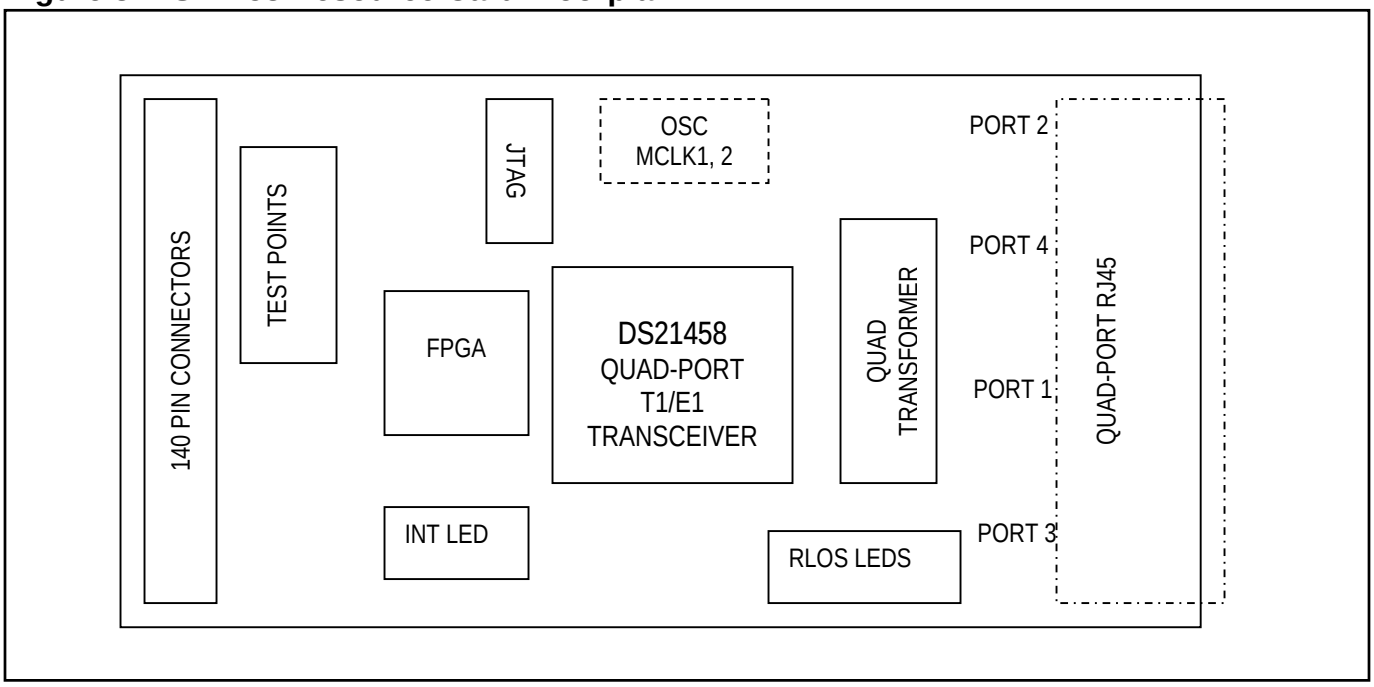
A 2-pin jumper, JP24, has been added to allow loopback. When installed, the board is in loopback at the CPLD; all traffic sent by the DS33Z44 is then sent back to the Z44. Traffic sent by the DS3174 is ignored in CPLD loopback mode.

The quad T3/E3 board is intended to be connected to the DS33Z11 or DS33Z44 motherboards. The quad T3/E3 board can be used with the quad T1/E1 board. When used in this manner, the quad T1/E1 board is stacked underneath the quad T3/E3 board. Jumpers on the T3/E3 board are then used to tri-state or enable individual ports on either board.

Figure 3 shows the DS21458 quad T1/E1 PC board floorplan. The current configuration is to populate oscillators for MCLK1 with a 2.048MHz oscillator. Testpoints for port 3 and port 4 are provided on the WAN card, and testpoints for ports 1 and 2 are provided on the motherboard.

The quad T1/E1 board can be used with the quad T3/E3 board. When used in this manner, the quad T1/E1 board is stacked underneath the quad T3/E3 board. Jumpers on the T3/E3 board are then used to tri-state or enable individual ports on either board.

Figure 3. DS21458 Resource Card Floorplan



PC BOARD ERRATA

- Silk screen for the serial resource card has V_{CC} and ground indicators pointing the wrong direction for configuration switches SW27, SW28, and SW32. This should be corrected with an adhesive label.
- Signal descriptions for JTAG connector are incorrect on the Quad T1E1 card. This should be corrected with an adhesive label.
- In the PCB layout the transformer TX primary is on the wrong side (creating a 2:1 winding instead of a 1:2). This has been corrected in the schematic, the PCB / assembly has been modified to correct this.

FILE LOCATIONS

This design kit relies upon several supporting files, which are provided on the CD and are available as a zip file from the Maxim website at www.maxim-ic.com/DS33Z44DK.

All locations are given relative to the top directory of the CD/zip file.

- DS33Z44 register definition files and configuration files:
  - .\cfg_demo_gui\DS33Z44_cfg_demo_gui\DS33Z44.def
  - .\DS33Z44_cfg_demo_gui\SU_LI_PORT4.def (def files for port 3, 2, 1 not shown)
  - .\DS33Z44_cfg_demo_gui\basic_config.mfg
- DS21458 register definition files and configuration files:
  - .\DS33Z44_cfg_demo_gui\Qt1e1_DS21458\DS21458RC.def
  - .\DS33Z44_cfg_demo_gui\Qt1e1_DS21458\DS21458RC_FPGA.def
  - .\DS33Z44_cfg_demo_gui\Qt1e1_DS21458\e1_gapclk_crc4_hdb3_nocas.ini
  - .\DS33Z44_cfg_demo_gui\Qt1e1_DS21458\gapclk_DS21458_T1_ESF_LBO0.ini
- DS3174 register definition files and configuration files:
  - .\DS33Z44_cfg_demo_gui\Qt3e3_DS3184\ds3184_evbrd_reduced.def
  - ….. 14 other low level def files ….
  - .\DS33Z44_cfg_demo_gui\Qt3e3_DS3184\84_t3_sct_needscoaxlb.mfg

BASIC OPERATION

Powering Up the Design Kit

- Attach resource card to main board.
- Connect PCB 3.3V and GND banana plugs to power supply. At power-up the system should draw approximately 1A.
- Set switches for software mode as described in Table 2 (short description follows).
  - Top left bank: All low, except for MODEC0, which is high.
  - Top right bank: A2, A1, A0 in mid position, SCANTRI low
  - Bottom Bank: All high (AFCS, FULLDS, H1OS)

General

- Upon power-up, the processor FPGA Status LEDs (DS19 green) will be lit. Interrupt LEDs (DS42 red) will not be lit. DS33Z44 Queue overflow LEDs (DS45, DS46, DS47, DS48 red) will not be lit. PHY LINK LED (DS02, DS03, DS14 green) should be lit if the Ethernet is connected.

Following are several basic system initializations.

Basic DS33Z44 Initialization (Used for All Quick Setups)

This section covers four basic methods for configuring the Z44. Any one of these initializations can be used with the following Quick Setup examples:

1. Upon power-up, the on-board device driver provides a basic configuration for the DS33Z44 and attached serial cards. This enables traffic to pass from the Ethernet port to the serial port. Consult the device driver documentation for further details. Device driver behavior is dependant upon jumper settings, which are detailed in Table 2.
2. Register-Based Configuration. Launch ChipView.exe and select *Register View.* When prompted for a definition file, pick the file named **DS33Z44.def**. After the definition file loads, go to the File menu and select File→Memory Config File→Load .MFG file. When prompted, select the file named **4Portsbasic_config.mfg**.
3. Hardware Mode. Set switches as described in the section for powering up the design kit, then change the following: HWMODE←3.3V, A0←3.3VV, A1←3.3V, A2←0V. This sets the part for LSB first, scrambling off, HDLC encapsulated. At this point traffic will pass from the Ethernet port to the serial port. In this mode broadcast frames are not passed (i.e., ping).
4. EEPROM mode is available with the DK, but is beyond the scope of this manual.

Quick Setup #1 (Device Driver + CPLD Loopback)

- On the serial resource card install jumper 24. Jumpers JP16–JP19 should be set high. This places the card in CPLD loopback and enables all four ports as described in Table 3.
- Complete the hardware configuration and one of the basic DS33Z44 configurations as described in the previous section.
- Using a patch cable, connect the Ethernet connector to an ordinary PC, or network test equipment. This should cause the link LED to turn on.
- At this point any packets sent to the DS33Z44 are echoed back. Incoming packets (i.e., ping) should cause the RX LED to blink, after which the TX LED should also blink.
- To interact with the device driver select from the drop down menu:
  - Tools→Plugins→Load Plugins. When asked if DLLs have already registered select yes
  - Select Tools→Plugins→DS33Z44/11/41 Device Driver Demo
  - A new form called ‘Zchip Configuration’ pops up.
  - Preload basic configuration for the GUI by selecting File→Load Settings (in the ‘Zchip Configuration’ form). Select the file named ‘basic_Config.eset’

Quick Setup #2 (DS3174 T3E3)

- On the DS3174 serial resource card install jumper J24. Jumpers JP16–JP19 should be set high. This places the card in DS3174 mode and enables all four ports as described in Table 3.
- Complete the hardware configuration and one of the basic DS33Z44 configurations as previously described.
- Using a patch cable, connect the Ethernet connector to an ordinary PC, or network test equipment. This should cause the link LED to turn on.
- Launch ChipView.exe (or use existing session if it is already open) and select *Register View*. When prompted for a definition file, pick the file name **ds3184_evbrd_reduced.def**. After the definition file loads, go to the File menu and select File→Memory Config File→Load .MFG file. When prompted, select the file named **84_t3_sct_needscoaxlb.mfg**.
- Place a loopback connector at the DS3174 network side.
- At this point, any packets sent to the DS33Z44 are echoed back. Incoming packets (i.e., ping) should cause the RX LED to blink, after which the TX LED should also blink.

Quick Setup #3 (DS21458 T1E1)

- Complete the hardware configuration and one of the basic DS33Z44 configurations as previously described.
- Using a patch cable, connect the Ethernet connector to an ordinary PC, or network test equipment. This should cause the link LED to turn on.
- Launch ChipView.exe (or use existing session if it is already open) and select *Register View.* When prompted for a definition file, pick the file named **DS21458.def**. After the definition file loads, go to the File menu and select File→Reg Ini File→Load Ini File. When prompted, pick the file named **e1_gapclk_crc4_hdb3_nocas.ini**.
- Place a loopback connector at the DS21458 network side; RLOS LED should go out.
- At this point any packets sent to the DS33Z44 are echoed back. Incoming packets (i.e. ping) should cause the RX LED to blink, after which the TX LED should also blink.

CONFIGURATION SWITCHES AND JUMPERS

The DS33Z44DK has several configuration switches, banana plugs, oscillators, and jumpers. Table 2 provides a description of these signals, given in order of appearance on the PC board (going from left to right, top to bottom).

Table 2. Main Board PC Board Configuration

SILKSCREEN REFERENCE	FUNCTION	BASIC SETTING		DESCRIPTION
		SW MODE	HW MODE	
J25.9 + J25.10	Reserved	Not Installed	—	This jumper is not for use with the DS33Z44 design kit. Pin J25.10 has been removed to prevent accidental installation.
J25.7 + J25.8	Enable device driver	User decision	—	When installed the device driver will configure the DS33Z44 and the Transceiver during power-up.
J25.5 + J25.6	Enable callbacks	User decision	—	When installed the driver will respond to interrupts.
GROUND (banana plug)	Power supply ground	—	—	System Ground. Always connected to power supply.
VDD 3.3V (banana plug)	Power supply VDD	—	—	System VDD. Always connected to power supply.
OnCe	BDM	—	—	Debug connector for processor
DCEDTES (3pos switch)	DS33Z44 mode pin; DTE/DCE selection	Low	Low	Low for DTE
RMIIMII (3pos switch)	DS33Z44 mode pin	Low	Low	High for RMII, low for MII
CKPHA (3pos switch)	DS33Z44 mode pin	Low	Low	SPI EEPROM hardware mode configuration switch
MODEC0 (3pos switch)	DS33Z44 mode pin	High	Low	Software mode selected
MODEC1 (3pos switch)	DS33Z44 mode pin	Low	Low	Software mode selected
HWMODE (3pos switch)	DS33Z44 mode pin	Low	Low	Hardware/software mode (software mode selected)
SCANMO (3pos switch)	DS33Z44 mode pin	Low	Low	Set low for normal operation
SCANTRI (3pos switch)	DS33Z44 mode pin	Low	Low	Set low for normal operation
….testpoints….	DS33Z44 testpoints	—	—	Processor bus, JTAG and LAN side testpoints for Zchip
Z-RESET (button)	DS33Z44 reset	—	—	System reset
A2, A1, A0 (3pos switches)	DS33Z44/SPI pins	Mid position	Mid position	Address pin/EEPROM config switch. Set to mid position to allow connection to processor.
SDRAM CLOCK	DS33Z44 SDRAM clock	Installed	Installed	100MHz oscillator to drive SDRAM clock
MII CLOCK	PHY MII clock	Installed	Installed	25MHz oscillator to drive SDRAM clock
spi_cs, spi_ck, spi_miso, spi_mosi	—	—	—	SPI signals (for EEPROM memory)
….testpoints…..	DS33Z44 testpoints	—	—	DS33Z44 serial port testpoints
AFCS (1 per port)	DS33Z44 mode pin	HW mode only	High	Set high to enable auto flow control.

SILKSCREEN REFERENCE	FUNCTION	BASIC SETTING		DESCRIPTION
		SW MODE	HW MODE	
FULLDS (1 per port)	DS33Z44 mode pin	HW mode only	High	Set high to enable full duplex.
H10S (1 per port)	DS33Z44 mode pin	HW mode only	High	Set high to confg for 100Mb.
GROUND/VDD (banana plug)	Power supply ground/3.3V	—	—	Redundant connection to system power. Use plugs at either top or bottom of board.
VDD 3.3V (banana plug)	Power supply VDD	—	—	Redundant connection to system power. Use plugs at either top or bottom of board.

Table 3. DS3174 Serial Reference Card Jumper Settings

JUMPER SETTINGS	MODE	COMMENT
JP16	Port 4 tri-state (at CPLD)	When the middle pin of this 3 position jumper is set to VCC, the CPLD passes traffic from the DS3174 to the DS33Z44. When the pin is set low, the CPLD tri-states this port.
JP17	Port 2 tri-state (at CPLD)	When the middle pin of this 3 position jumper is set to VCC, the CPLD passes traffic from the DS3174 to the DS33Z44. When the pin is set low, the CPLD tri-states this port.
JP18	Port 3 tri-state (at CPLD)	When the middle pin of this 3 position jumper is set to VCC, the CPLD passes traffic from the DS3174 to the DS33Z44. When the pin is set low, the CPLD tri-states this port.
JP19	Port 1 tri-state (at CPLD)	When the middle pin of this 3 position jumper is set to VCC, the CPLD passes traffic from the DS3174 to the DS33Z44. When the pin is set low, the CPLD tri-states this port.
J243	CPLD loopback	CPLD loopback makes the following connections: Zrser ← Ztser, Ztden ← 3.3V, Zrden ← 3.3V, Ztclki ← OscY03, Zrclki ← OscY03

ADDRESS MAP (ALL CARDS)

Motorola resource card address space begins at 0x81000000. All offsets given below are relative to the beginning of the daughter card address space (shown previously).

Table 4. Overview of Daughter Card Address Map

OFFSET	DEVICE	DESCRIPTION
0X0000 to 0X0087	FPGA	Processor board identification
0X1000 to 0X1FFF	DS33Z44	DS33Z44. Uses CS_X1.
0X2000 to 0X2FFF	DS21458	T1E1 DS21458 resource card. Uses CS_X2.
0X4000 to 0X4010	FPGA	FPGA on DS21458 resource card. Used to facilitate IBO mode. Default configuration of FPGA is compatible with non-IBO mode functionality. The FPGA settings do not require modification for use with the DS33Z44.
0X3000 to 0X3FFF	DS3174	T3E3 resource card. Uses CS_X3.

Registers in the DS33Z44, DS21458, and DS3174 can be easily modified using the ChipView host-based user-interface software with the definition files previously mentioned.

DS33Z44 INFORMATION

For more information about the DS33Z44, consult the DS33Z44 data sheet available on our website at www.maxim-ic.com/DS33Z44.

DS33Z44DK INFORMATION

For more information about the DS33Z44DK, including software downloads, consult the DS33Z44DK data sheet available on the our website at www.maxim-ic.com/DS33Z44DK.

TECHNICAL SUPPORT

For additional technical support, go to www.maxim-ic.com/support.

DOCUMENT REVISION HISTORY

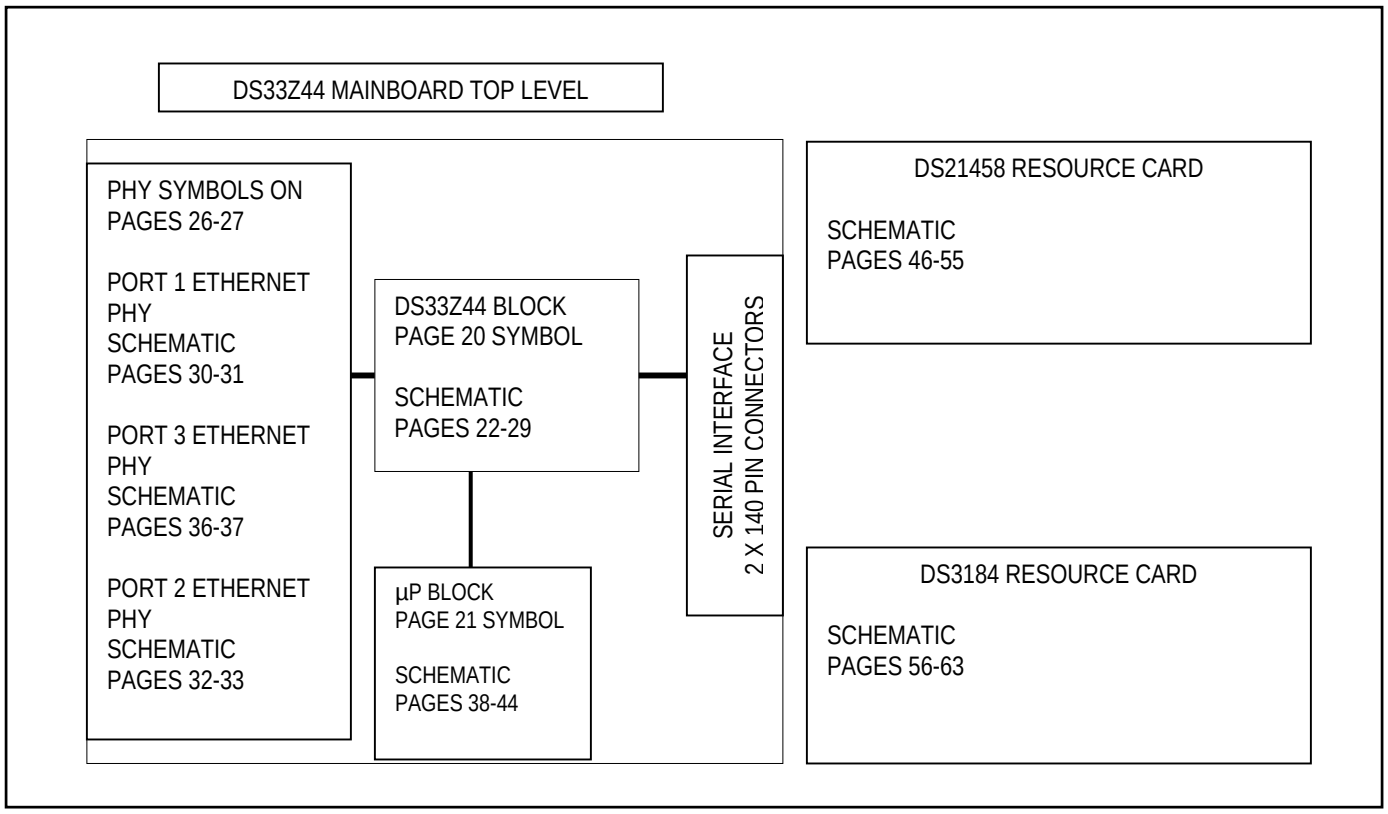
REVISION DATE	DESCRIPTION
032305	Initial DS33Z44DK data sheet release.
042205	Updated *Basic DS33Z44 Initialization* section; added step to *Quick Setup #1*.
051105	Added new PC board errata.
110106	Updated schematics.

SCHEMATICS

The DS33Z44DK schematics are featured in the following pages. As this is a hierarchal schematic some explanation is in order. The main board is composed of six hierarchal blocks: the processor block, the DS33Z44 block, and four Ethernet blocks inside the DS33Z44 block, which is a nested hierarchy block. Each serial card (DS21458 and DS3174) consists of a single hierarchy block, which connects to a 140-pin AV bus that snaps into the mainboard.

All signals inside a hierarchy block are local, with exception for V_{CC} and ground. In-port and out-port connectors are used to allow signals inside a hierarchy block to become accessible as pins on the hierarchy blocks symbol. From here, blocks are wired together as if they were ordinary components. The system diagram is shown again below, with schematic page numbers given for each functional block.

This system contained other hierarchy blocks that are not shown (primarily a single-port serial card and the DS33Z11 mainboard). Due to this, page numbers will not be continuous and some gaps in numbering will be seen when referring to the total page count. However, page numbers inside any given hierarchy block will be continuous.



CR-20 : @_ZTOP_LIB\._ZTOPDN_\(SCH_1):PAGE1_IB@_ZTOP_LIB\._Z44TOP_DN\(SCH_1):PAGE1

DS33Z44 TOP LEVEL

PLUG
P2 CONNECTOR (PLUG)

JB14

PLUG
P1 CONNECTOR (PLUG)

JB10

HIERARCHICAL BLOCK
_z44andlan_dn

PAGES 22-29

MOTHERBOARD CONNECTORS FOR WAN R.C.

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 1/2(BLOCK) 20/71(TOTAL)

BLOCK NAME: _z44top_dn. PARENT BLOCK: _ztopdn_\

PRINTED Fri Oct 20 11:06:56 2006

CR-21 : @_ZTOP_LIB\._ZTOPDN_\(SCH_1):PAGE1_IB@_ZTOP_LIB\._Z44TOP_DN\(SCH_1):PAGE2

I1

HIERARCHICAL BLOCK

_motprocrescard_dn

PAGES 38-44

38B7v 20C8<> 20C7<>	INT2	INT2	CS_X1	CS_X1	20D3< 42B3v
38B7v 20C7<>	INT3	INT3	CS_X2	CS_X2	20A5<> 42B3v
38B7v 20C7<>	INT4	INT4	CS_X3	CS_X3	20A5<> 42A4v
39D4v 20C8<>	INT5	INT5	CS_X4	CS_X4	20C3<> 42A4v
			CS_X5	CS_X5	20C5<> 42A4v
			RESET_B	RESET_B	20C7<> 20C3< 38A5v
42C3v 20D3<	RD_DUT	RD_DUT			
42C3v 20D3<	WR_DUT	WR_DUT			
42D5v 20D3<	D_DUT<7..0>	D_DUT<7..0>			
42A6v 42A5v 20D3<	A_DUT<11..0>	A_DUT<11..0>	RW_X	RW_X	20A3<> 42B3v
42C3v 20C1>	BIS0_DUT	BIS0_DUT	WR	WR_X	20A5<> 42B3v
42C3v 20C1>	BIS1_DUT	BIS1_DUT	XA<15..0>	XA<15..0>	20A6 20AB 42C7v
42C3v 20C1>	BTS_DUT	BTS_DUT	XD<7..0>	XD<7..0>	20A3 20A5 42B3v

TMS_NU TDI_NU TCK_NU TDO_NU

TMS_NU 20AB<> 44A7v
TDI_NU 20AB<> 44A7v
TCK_NU 20A7<> 44A7v
TDO_NU 20A7<> 44A7v

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 2/2 (BLOCK) 21/71 (TOTAL)

BLOCK NAME: _z44top_dn. PARENT BLOCK: _ztopdn_\

F7 JTMS 22A5<> — JTMS — JTAG
E4 JTDI 22A5<> — JTDI
E5 JTDO 22A5<> — JTDO
D4 JTCLK 22A5<> — JTCLK
E6 JTRST 22A5<> — JTRST

U22
DS33Z44_U1

MII/RMII

2BA4< REF_CLK — YTPB02 — C15 — REF_CLK
REF_CLKO — RB181 — B15 — REF_CLKO
27B3> 26B6> 26B3> 27B6> MDC — R99 — YTP34 — F11 — MDC
27B3> 26B6> 26B3> 27B6> MDIO — RB161 — YTPB01 — F10 — MDIO

SDRAM CONTROL

24B4< SD_BA0 — RB230 — R8 — SBA<0>
24B4< SD_BA1 — RB246 — R9 — SBA<1>
24C4< SD_DQM0 — R166 — T8 — SDMASK<0>
24C4< SD_DQM1 — RB239 — M7 — SDMASK<1>
24C4< SD_DQM2 — R147 — T11 — SDMASK<2>
24C4< SD_DQM3 — RB217 — N11 — SDMASK<3>
24C4< SD_CS — R158 — P8 — SDCS*
24C3< SD_CLKO — RB226 — T7 — SDCLKO
2BD5< SD_CLKI — T15 — SYSCLKI
24C4< SD_RAS — RB219 — P15 — SRAS*
24C4< SD_CAS — R163 — N7 — SCAS*
24C4< SD_WE — RB282 — R7 — SWE*

UNMARKED RESISTORS ARE 30 OHM

MICRO PORT/SPI MASTER PORT

INT* — INT D3 — OUT — 20D2^ 22A6<>
CS* — CS D1 — IN — 20D3^
SPI_CS* — SPICSZ E13 — IN — 22C2<
RD*/DS* — RD E1 — IN — 20D3^
WR*/RW* — WR E2 — IN — 20D3^
RST* — RESET_B D8 — IN
HWMODE — HWMODE D5 — OUT — 2BD4< 20C2^
MODEC<0> — MODEC0 D6 — OUT — 2BD2< 20C2^
MODEC<1> — MODEC1 D4 — OUT — 2BD4< 20C2^
DCEDTES — DCEDTES S1 — 2BD2<
RMIIMIIS — RMIIMIIS C4 — 2BC4<
SCAN ENABLE — SCANEN E7 — 2BB4<
SCAN MODE — SCANMOD B3 — 2BC4<
CKPHA — CKPHA G4 — 2BB4<

A<0> A1 ZADDR0 22B2<>
A<1> B1 ZADDR1 22B2<>
A<2> A2 ZADDR2 22A2<>
A<3> B2 3
A<4> C2 4
A<5> A3 5
A<6> B3 6
A<7> C3 7
A<8> A4 8
A<9> B4 9 — ADDR<9..0> IN 20D3^ 22B1<

D<0>/MOSI A5 ZMOSI 0
D<1>/MISO A6 ZMISO 1
D<2>/SPICK A7 ZSPISCK 2
D<3> B5 3
D<4> B6 4
D<5> B7 5
D<6> C5 6
D<7> C6 7 — DAT<7..0> IO 20D3^

2.7V
Y02
22C4<> ZMOSI 5 SI — VCC 8 — V3_3
22C4<> ZMISO 2 SO — WP* 3 — RB79 10K
22B4<> ZSPISCK 6 SCK — HOLD* 7 — RB74 10K
22A6> ZSPICS 1 CS* — GND 4
AT25160A_U

V3_3
SW04 SP3T — 22D4< ZADDR0 — 0
SW08 SP3T — 22C4< ZADDR1 — 1
SW18 SP3T — 22C4< ZADDR2 — 2
4
IN — 20D3^ 22C4< — ADDR<9..0>

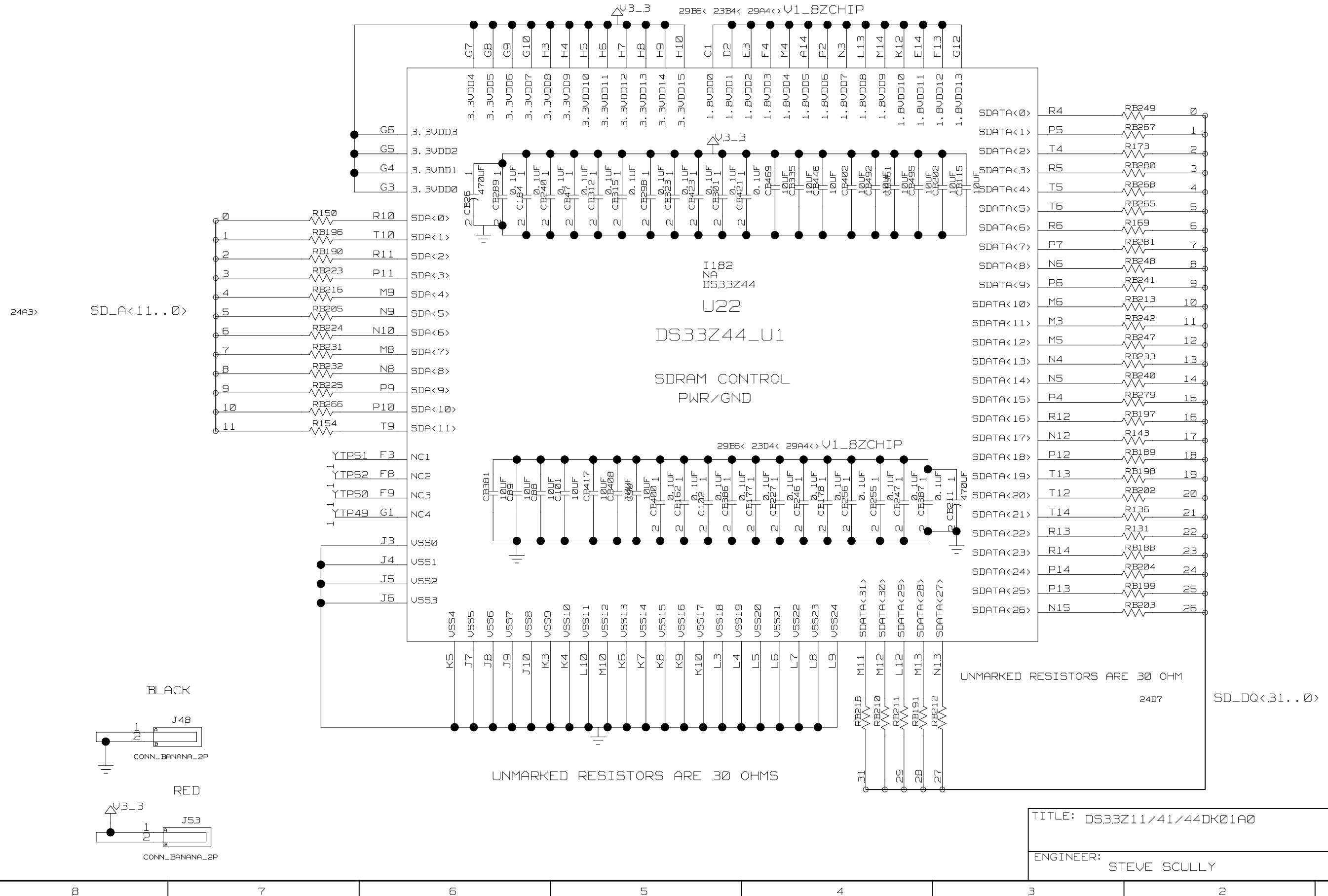
V3_3 — RB332 330 — 1 2 — RED — DS42
NC7SZ86_U BUFFER — U2B07 — 4 1 — INT — 22A7> 20D2^

J32
22D6< JTCLK 1 — 1 2 — 2 TCK_NU
22D6< JTMS 3 — 3 4 — 4 TMS_NU
22D6<> JTDO 5 — 5 6 — 6 TDI_NU
22D6< JTDI 7 — 7 8 — 8 TDO_NU
22D6< JTRST 9 — 9 10 — 10 — V3_3
CONN_10P

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:1/8(BLOCK) 22/71(TOTAL)

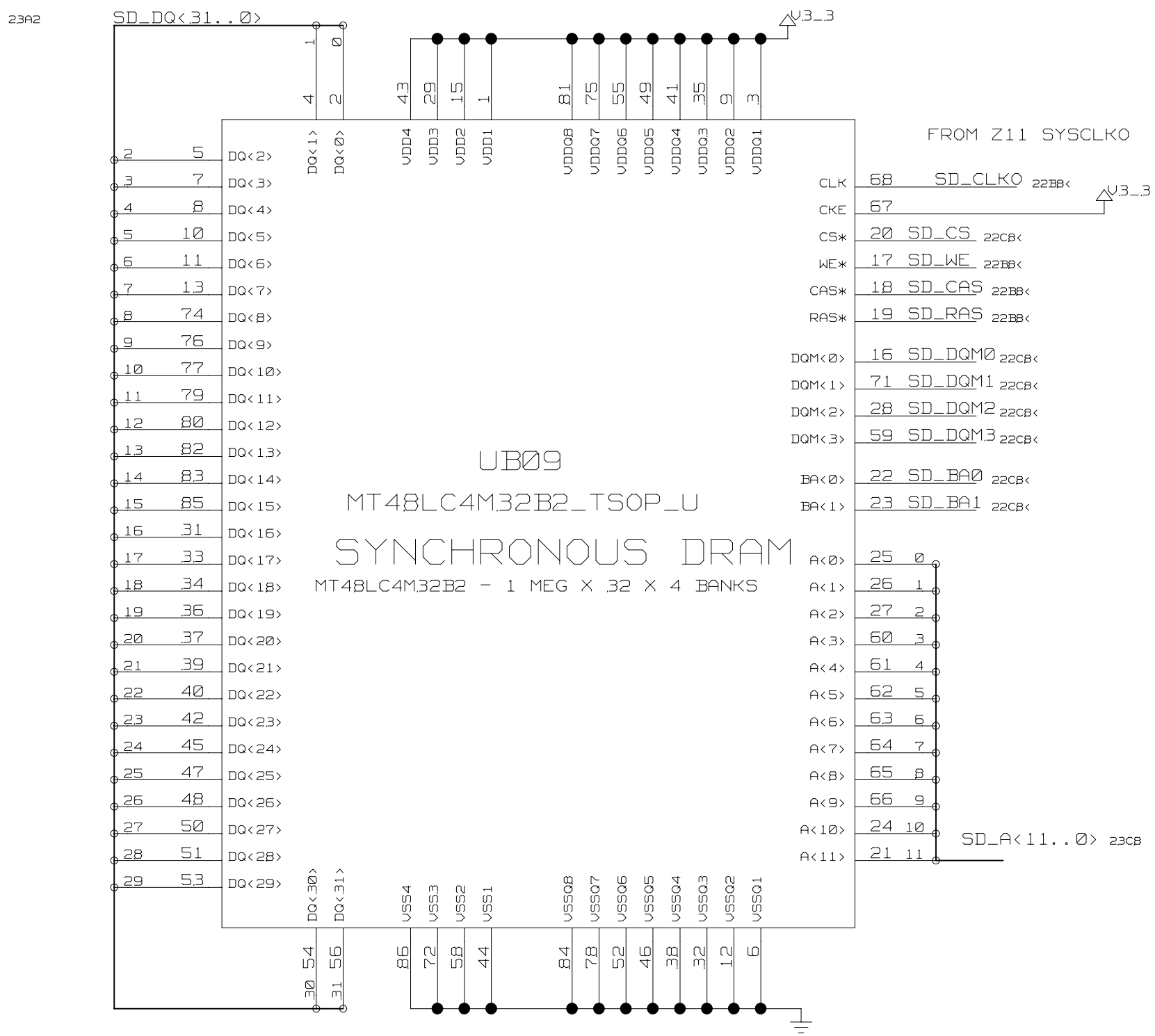
BLOCK NAME: _z44andlan_dn. PARENT BLOCK: _z44top_dn\

CR-23 : @_ZTOP_LIB\._ZTOPDN_\(SCH_1):PAGE1_IB@_ZTOP_LIB\._Z44TOP_DN\(SCH_1):PAGE1_I2@_ZTOP_LIB\._Z44ANDLAN_DN\(SCH_1):PAGE2



TITLE: DS.3.3Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:2/8(BLOCK) 23/71(TOTAL)

BLOCK NAME: _z44andlan_dn. PARENT BLOCK: _z44top_dn\



TITLE: DS.3.3Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:3/8(BLOCK) 24/71(TOTAL)

CR-25 : @_ZTOP_LIB\._ZTOPDN_\(SCH_1):PAGE1_IB@_ZTOP_LIB\._Z44TOP_DN\(SCH_1):PAGE1_I2@_ZTOP_LIB\._Z44ANDLAN_DN\(SCH_1):PAGE4

REV01A0 SCHEMATIC SYMBOL (AND PCB) FOR Z44 HAD ERRORS
TXD/RXD PINS FOR PHY CONNECTION WERE INCORRECT
CORRECT PINOUT SHOWN AT BOTTOM OF PAGE

U22

PORT1 PIN G2

DS33Z44_U1

20D2^ IN	RCLKI<1> YTP57	G2	RCLKI	PORT	TCLKI	F1 YTP63	TCLKI<1>	IN 20D2^
20D2^ IN	RSER<1> YTP59	H1	RSER		TSER	F2 YTP65	RB335 30 TSER<1>	OUT 20D2^
20D2^ IN	RDEN<1> YTP58	H2	RDEN/RBSYNC		TDEN/TBSYNC	F5 YTP64	TDEN<1>	IO 20D2^
26D5>	RXD0<1>	B11	RXD0		TXD0	B9	R105 30 TXD0<1>	26DB<
26D5>	RXD1<1>	C11	RXD1		TXD1	C9	R122 30 TXD1<1>	26DB<
26D5>	RXD2<1>	D11	RXD2		TXD2	D9	R96 30 TXD2<1>	26DB<
26D5>	RXD3<1>	E11	RXD3		TXD3	E9	R115 30 TXD3<1>	26DB<
26C5>	RXDV<1>	D10	RXDV		TX_EN	E10	R98 30 TX_EN<1>	26CB<
26C5>	RX_CRS<1>	D12	RX_CRS/CRS_DV		TX_CLK	A9	TX_CLK<1>	26DB<
26C5>	RX_ERR<1>	E12	RX_ERR		RX_CLK	A11	RX_CLK<1>	26D5>
					QOVF	C7	QOVF<1>	29DB<>
26C5>	COL_DET<1>	D13	COL_DET		H10S	B10	H10S<1>	29C2<
29D2<	FULLDS<1>	A10	FULLDS		AFCS	C10	AFCS<1>	29D2<

U22

PORT2 PIN L2

DS33Z44_U1

20D2^ IN	RCLKI<2> YTP54	L2	RCLKI	PORT	TCLKI	J1 YTP60	TCLKI<2>	IN 20D2^
20D2^ IN	RSER<2> YTP56	K1	RSER		TSER	J2 YTP62	RB33930 TSER<2>	OUT 20D2^
20D2^ IN	RDEN<2> YTP55	L1	RDEN/RBSYNC		TDEN/TBSYNC	K2 YTP61	TDEN<2>	IO 20D2^
26D2>	RXD0<2>	K13	RXD0		TXD0	R15	RB164 TXD0<2>	26D5<
26D2>	RXD1<2>	K14	RXD1		TXD1	R16	RB165 30 TXD1<2>	26D5<
26D2>	RXD2<2>	H15	RXD2		TXD2	L15	RB180 30 TXD2<2>	26D5<
26D2>	RXD3<2>	K16	RXD3		TXD3	N14	RB121 30 TXD3<2>	26D5<
26C2>	RXDV<2>	K15	RXDV		TX_EN	L14	RB179 30 TX_EN<2>	26C5<
26C2>	RX_CRS<2>	N16	RX_CRS/CRS_DV		TX_CLK	M16	TX_CLK<2>	26D5<
26C2>	RX_ERR<2>	T16	RX_ERR		RX_CLK	L16	RX_CLK<2>	26D2>
					QOVF	C8	QOVF<2>	29DB<>
26C2>	COL_DET<2>	P16	COL_DET		H10S	L11	H10S<2>	29A2<
29B2<	FULLDS<2>	J15	FULLDS		AFCS	J16	AFCS<2>	29B2<

U22

PORT3 PIN N2

DS33Z44_U1

20D2^ IN	RCLKI<3>	N2	RCLKI	PORT	TCLKI	M1	TCLKI<3>	IN 20D2^
20D2^ IN	RSER<3>	P1	RSER		TSER	M2	RB311 30 TSER<3>	OUT 20D2^
20D2^ IN	RDEN<3>	N1	RDEN/RBSYNC		TDEN/TBSYNC	P3	TDEN<3>	IO 20D2^
27D5>	RXD0<3>	G15	RXD0		TXD0	F15	R97 30 TXD0<3>	27DB<
27D5>	RXD1<3>	J14	RXD1		TXD1	G14	R123 30 TXD1<3>	27DB<
27D5>	RXD2<3>	J13	RXD2		TXD2	H13	RB187 30 TXD2<3>	27DB<
27D5>	RXD3<3>	J12	RXD3		TXD3	H14	RB169 30 TXD3<3>	27DB<
27C5>	RXDV<3>	K11	RXDV		TX_EN	E15	RB170 30 TX_EN<3>	27CB<
27C5>	RX_CRS<3>	M15	RX_CRS/CRS_DV		TX_CLK	G16	TX_CLK<3>	27DB<
27C5>	RX_ERR<3>	G11	RX_ERR		RX_CLK	H16	RX_CLK<3>	27D5>
					QOVF	B8	QOVF<3>	29CB<>
27C5>	COL_DET<3>	H11	COL_DET		H10S	F12	H10S<3>	29C4<
29D4<	FULLDS<3>	H12	FULLDS		AFCS	J11	AFCS<3>	29C4<

U22

PORT4 PIN T3

DS33Z44_U1

20D2^ IN	RCLKI<4>	T3	RCLKI	PORT	TCLKI	R1	TCLKI<4>	IN 20D2^
20D2^ IN	RSER<4>	T2	RSER		TSER	R2	RB320 30 TSER<4>	OUT 20D2^
20D2^ IN	RDEN<4>	T1	RDEN/RBSYNC		TDEN/TBSYNC	R3	TDEN<4>	IO 20D2^
27D2>	RXD0<4>	B13	RXD0		TXD0	B16	R126 30 TXD0<4>	27D4<
27D2>	RXD1<4>	C13	RXD1		TXD1	C16	RB171 30 TXD1<4>	27D4<
27D2>	RXD2<4>	B14	RXD2		TXD2	D16	RB167 30 TXD2<4>	27D4<
27D2>	RXD3<4>	C14	RXD3		TXD3	E16	RB168 30 TXD3<4>	27D4<
27C2>	RXDV<4>	D15	RXDV		TX_EN	G13	R124 30 TX_EN<4>	27C4<
27C2>	RX_CRS<4>	F14	RX_CRS/CRS_DV		TX_CLK	A16	TX_CLK<4>	27D4<
27C2>	RX_ERR<4>	D14	RX_ERR		RX_CLK	A13	RX_CLK<4>	27D2>
					QOVF	A8	QOVF<4>	29CB<>
27C2>	COL_DET<4>	F16	COL_DET		H10S	B12	H10S<4>	29A4<
29B4<	FULLDS<4>	A12	FULLDS		AFCS	C12	AFCS<4>	29A4<

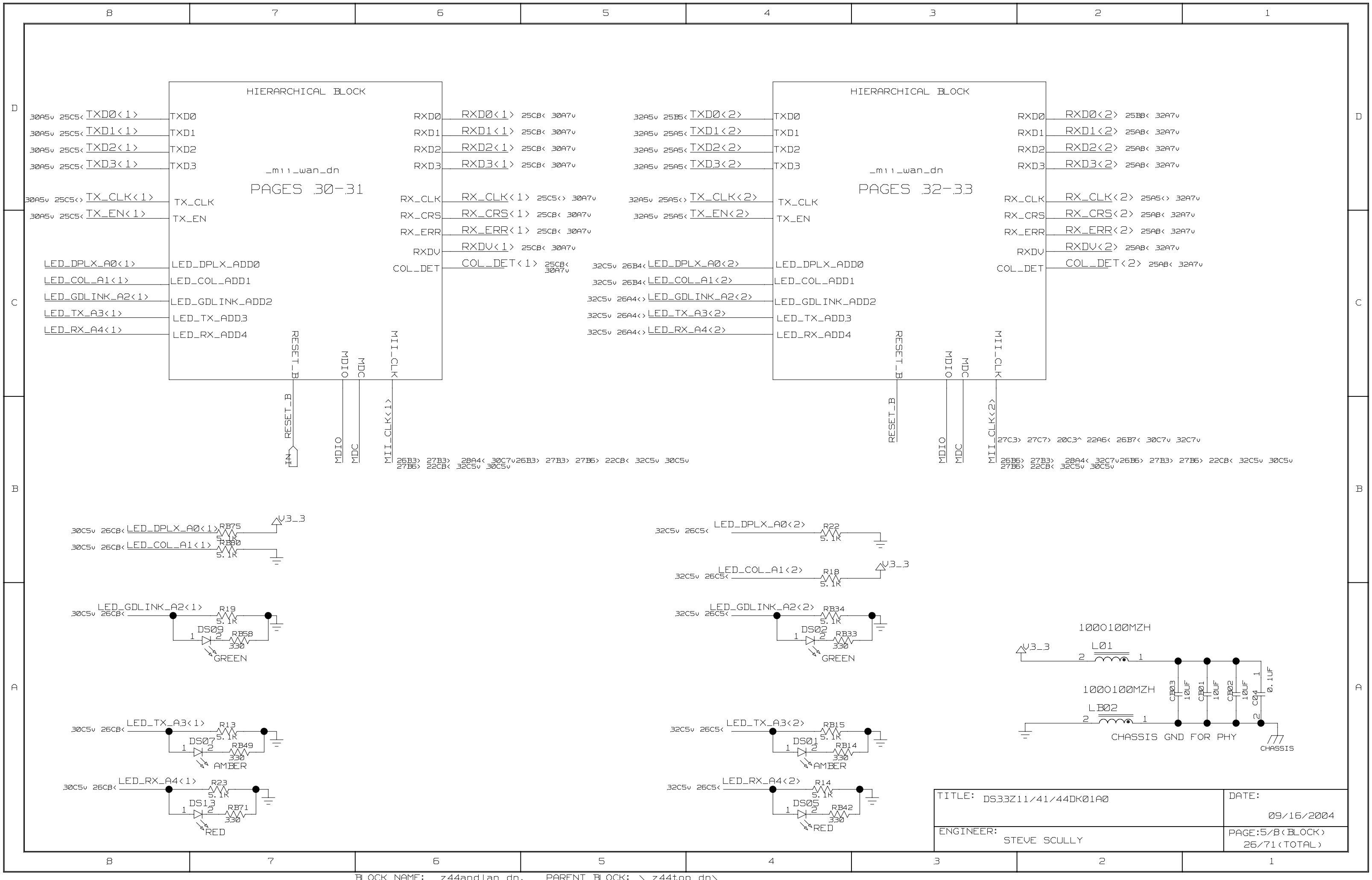
PORT1 TXD0--TXD3 B9, C9, D9, E9
PORT2 TXD0--TXD3 R15, R16, L15, N14
PORT3 TXD0--TXD3 F15, G14, H13, H14
PORT4 TXD0--TXD3 B16, C16, D16, E16

PORT1 RXD0--RXD3 B11, C11, D11, E11
PORT2 RXD0--RXD3 K13, K14, H15, K16
PORT3 RXD0--RXD3 G15, J14, J13, J12
PORT4 RXD0--RXD3 B13, C13, B14, C14

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 4/8 (BLOCK) 25/71 (TOTAL)

BLOCK NAME: _z44andlan_dn. PARENT BLOCK: _z44top_dn\

CR-26 : @_ZTOP_LIB\._ZTOPDN_\(SCH_1):PAGE1_IB@_ZTOP_LIB\._Z44TOP_DN\(SCH_1):PAGE1_I2@_ZTOP_LIB\._Z44ANDLAN_DN\(SCH_1):PAGE5



TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:5/8(BLOCK) 26/71(TOTAL)

BLOCK NAME: _z44andlan_dn PARENT BLOCK: _z44top_dn\

CR-27 : @_ZTOP_LIB\._ZTOPDN_\(SCH_1):PAGE1_IB@_ZTOP_LIB\._Z44TOP_DN\(SCH_1):PAGE1_I2@_ZTOP_LIB\._Z44ANDLAN_DN\(SCH_1):PAGE5

HIERARCHICAL BLOCK

_mii_wan_dn

PAGES 36-37

TXD0 ← 36A5v 25C1< TXD0<3>
TXD1 ← 36A5v 25C1< TXD1<3>
TXD2 ← 36A5v 25C1< TXD2<3>
TXD3 ← 36A5v 25C1< TXD3<3>
TX_CLK ← 36A5v 25C1<> TX_CLK<3>
TX_EN ← 36A5v 25C1< TX_EN<3>
LED_DPLX_ADD0 ← 27B8< 36C5v LED_DPLX_A0<3>
LED_COL_ADD1 ← 27B8< 36C5v LED_COL_A1<3>
LED_GDLINK_ADD2 ← LED_GDLINK_A2<3>
LED_TX_ADD3 ← LED_TX_A3<3>
LED_RX_ADD4 ← LED_RX_A4<3>

RXD0 → RXD0<3> 25C4< 36A7v
RXD1 → RXD1<3> 25C4< 36A7v
RXD2 → RXD2<3> 25C4< 36A7v
RXD3 → RXD3<3> 25C4< 36A7v
RX_CLK → RX_CLK<3> 25C1<> 36A7v
RX_CRS → RX_CRS<3> 25C4< 36A7v
RX_ERR → RX_ERR<3> 25C4< 36A7v
RXDV → RXDV<3> 25C4< 36A7v
COL_DET → COL_DET<3> 25C4< 36A7v

RESET_B → RESET_B
MDIO → MDIO
MDC → MDC
MII_CLK → MII_CLK<3>

26B3> 26B6> 28A4< 36C7v 26B3> 26B6> 27B3> 22C8< 34C5v 36C5v
27B3> 22C8< 34C5v 36C5v

HIERARCHICAL BLOCK

_mii_wan_dn

PAGES 34-35

TXD0 ← 34A5v 25B1< TXD0<4>
TXD1 ← 34A5v 25B1< TXD1<4>
TXD2 ← 34A5v 25A1< TXD2<4>
TXD3 ← 34A5v 25A1< TXD3<4>
TX_CLK ← 34A5v 25A1<> TX_CLK<4>
TX_EN ← 34A5v 25A1< TX_EN<4>
LED_DPLX_ADD0 ← 34C5v 27B4< LED_DPLX_A0<4>
LED_COL_ADD1 ← 34C5v 27B4< LED_COL_A1<4>
LED_GDLINK_ADD2 ← 34C5v 27A4<> LED_GDLINK_A2<4>
LED_TX_ADD3 ← 34C5v 27A4<> LED_TX_A3<4>
LED_RX_ADD4 ← 34C5v 27A4<> LED_RX_A4<4>

RXD0 → RXD0<4> 25B4< 34A7v
RXD1 → RXD1<4> 25B4< 34A7v
RXD2 → RXD2<4> 25A4< 34A7v
RXD3 → RXD3<4> 25A4< 34A7v
RX_CLK → RX_CLK<4> 25A1<> 34A7v
RX_CRS → RX_CRS<4> 25A4< 34A7v
RX_ERR → RX_ERR<4> 25A4< 34A7v
RXDV → RXDV<4> 25A4< 34A7v
COL_DET → COL_DET<4> 25A4< 34A7v

RESET_B → RESET_B
MDIO → MDIO
MDC → MDC
MII_CLK → MII_CLK<4>

26B3> 27C7> 20C3^ 22A6< 26B7< 36C7v 34C7v
26B3> 26B6> 28A4< 34C7v 26B3> 26B6> 27B6> 22C8< 34C5v 36C5v
27B6> 22C8< 34C5v 36C5v

36C5v 27C8< LED_DPLX_A0<3> RB82 5.1K → V3_3
36C5v 27C8< LED_COL_A1<3> RB51 5.1K → V3_3

LED_GDLINK_A2<3> 36C5v 27C8< RB32 5.1K
DS03 1 2 RB40 330 GREEN

LED_TX_A3<3> 36C5v 27C8< RB62 5.1K
DS12 1 2 RB77 330 AMBER

LED_RX_A4<3> 36C5v 27C8< RB36 5.1K
DS04 1 2 RB43 330 RED

34C5v 27C5< LED_DPLX_A0<4> R30 5.1K
34C5v 27C5< LED_COL_A1<4> R29 5.1K

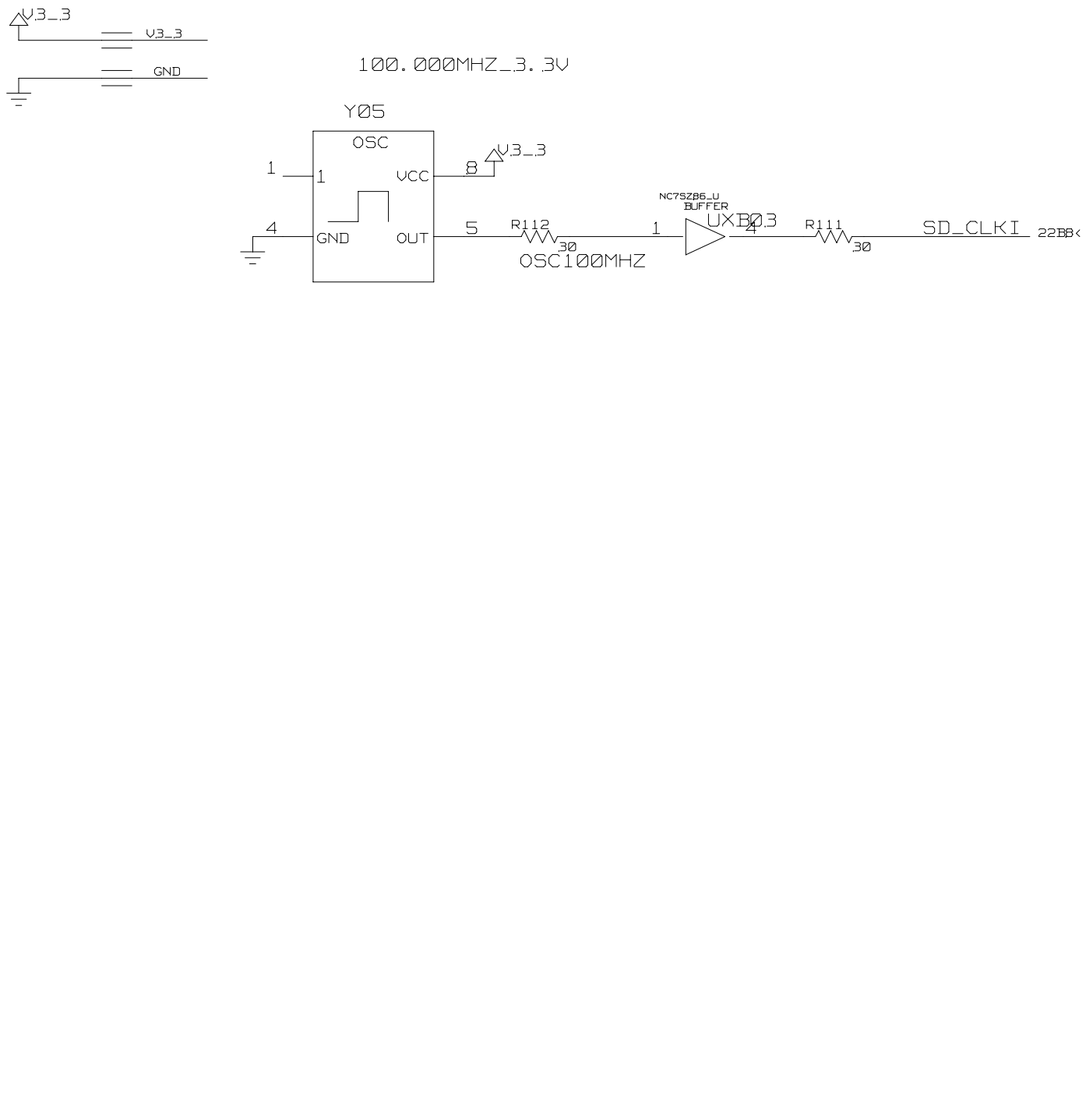
LED_GDLINK_A2<4> 34C5v 27C5< RB73 5.1K → V3_3
GREEN R24 330 DS14

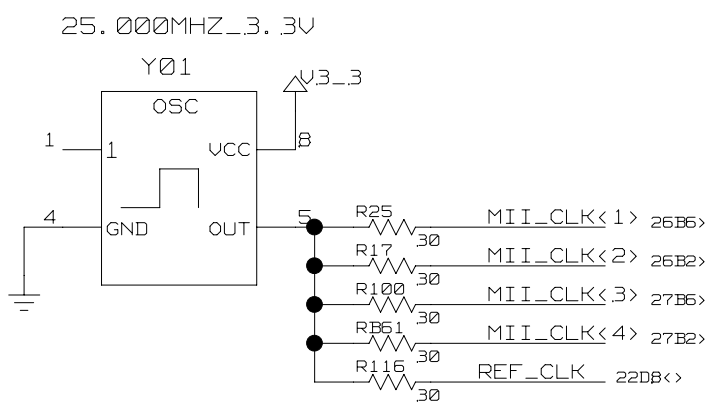
LED_TX_A3<4> 34C5v 27C5< R20 5.1K
DS10 1 2 RB59 330 AMBER

LED_RX_A4<4> 34C5v 27C5< R15 5.1K
DS08 1 2 RB53 330 RED

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:6/8(BLOCK) 27/71(TOTAL)

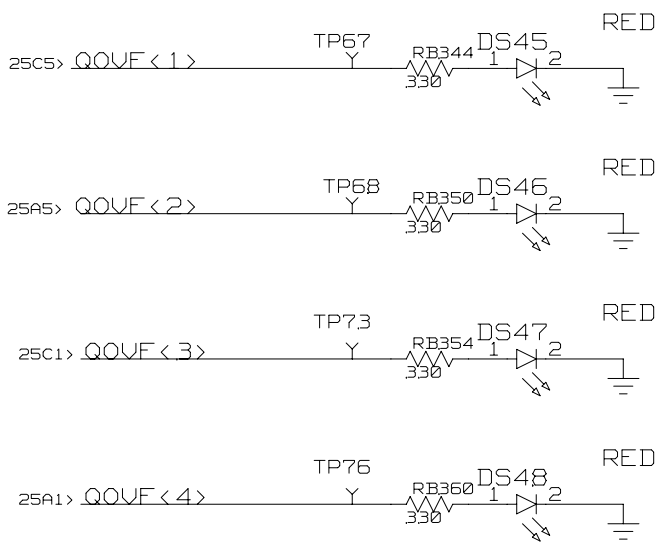
BLOCK NAME: _z44andlan_dn, PARENT BLOCK: _z44top_dn\

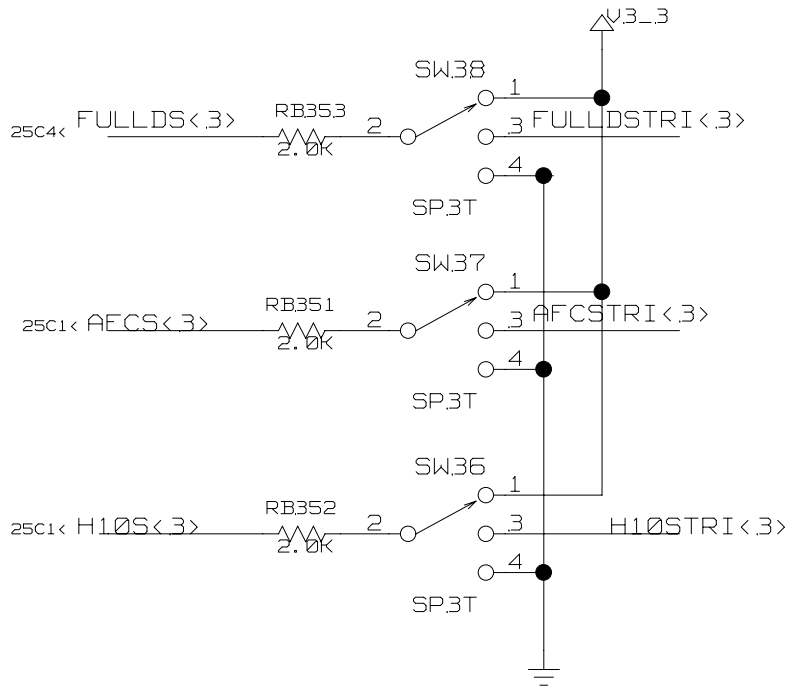


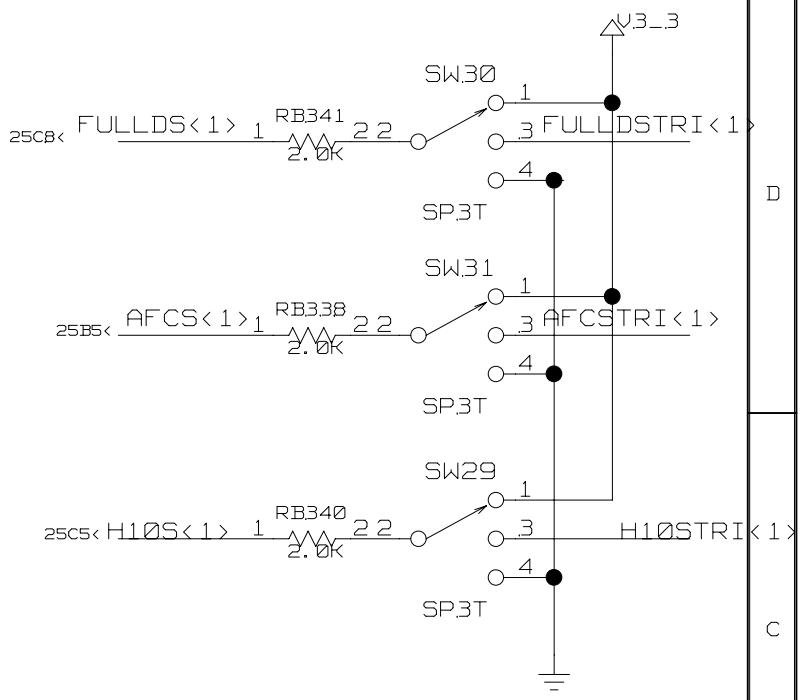


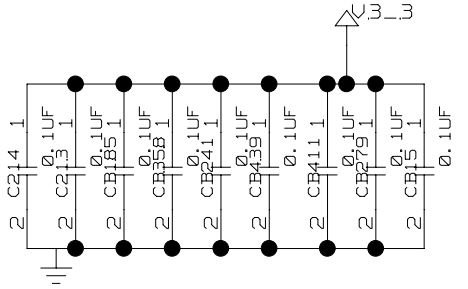
TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 7/8 (BLOCK) 28/71 (TOTAL)

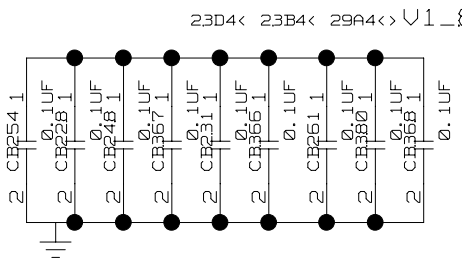
CR-29 : @_ZTOP_LIB\._ZTOPDN_\(SCH_1):PAGE1_IB@_ZTOP_LIB\._Z44TOP_DN\(SCH_1):PAGE1_I2@_ZTOP_LIB\._Z44ANDLAN_DN\(SCH_1):PAGE8

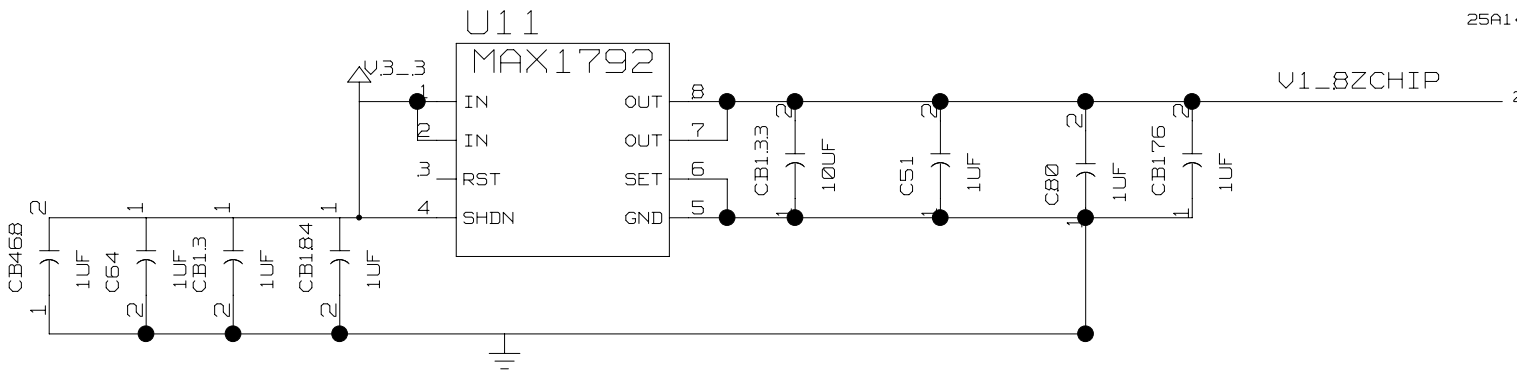


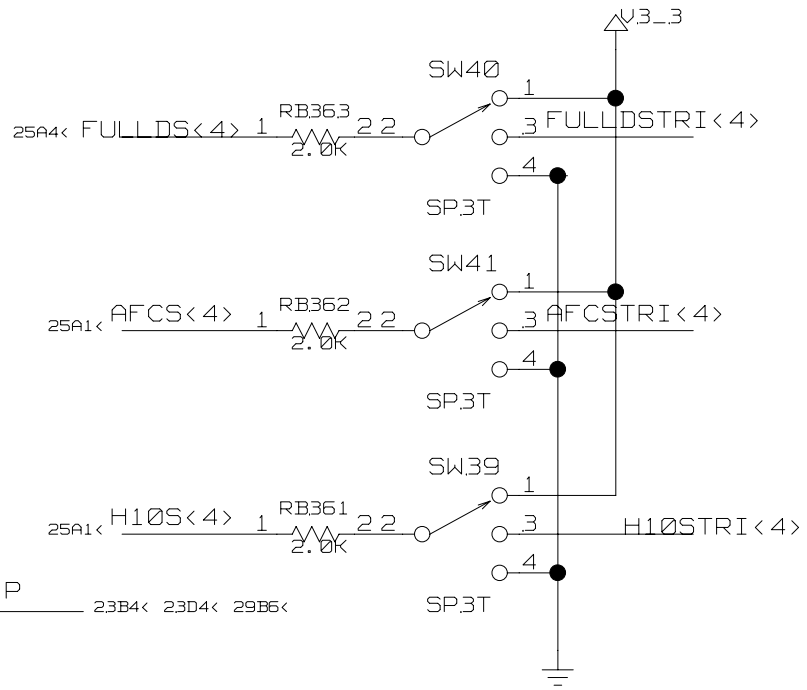


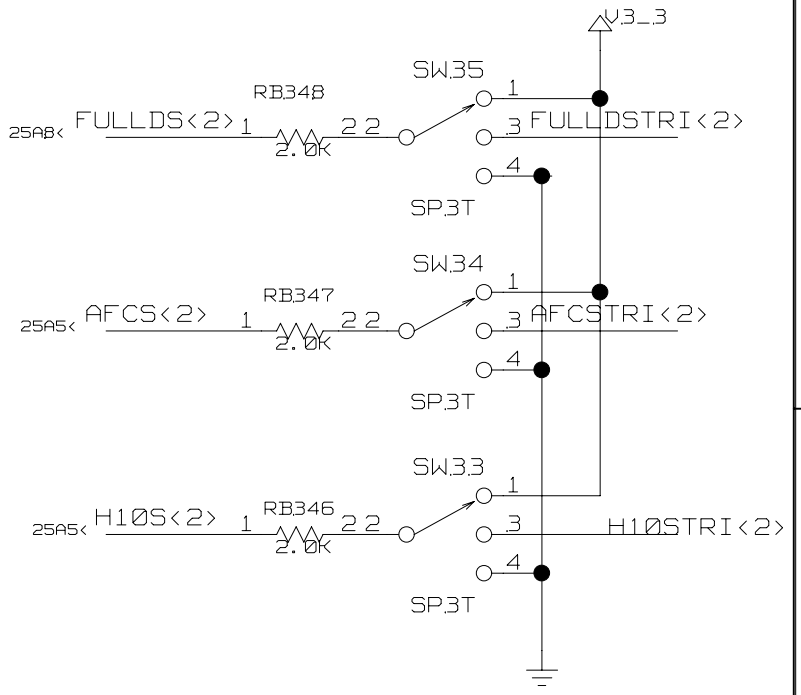








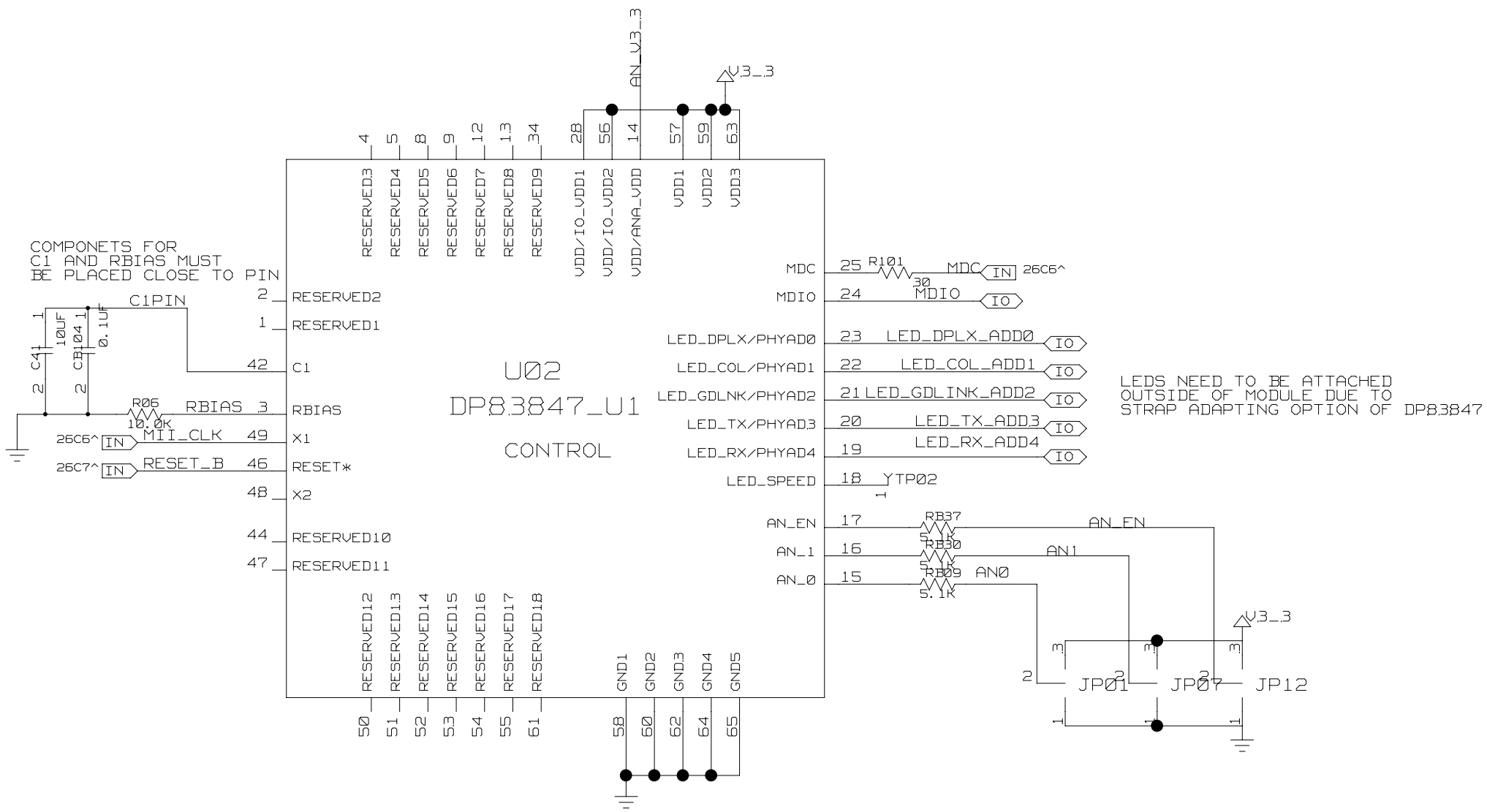


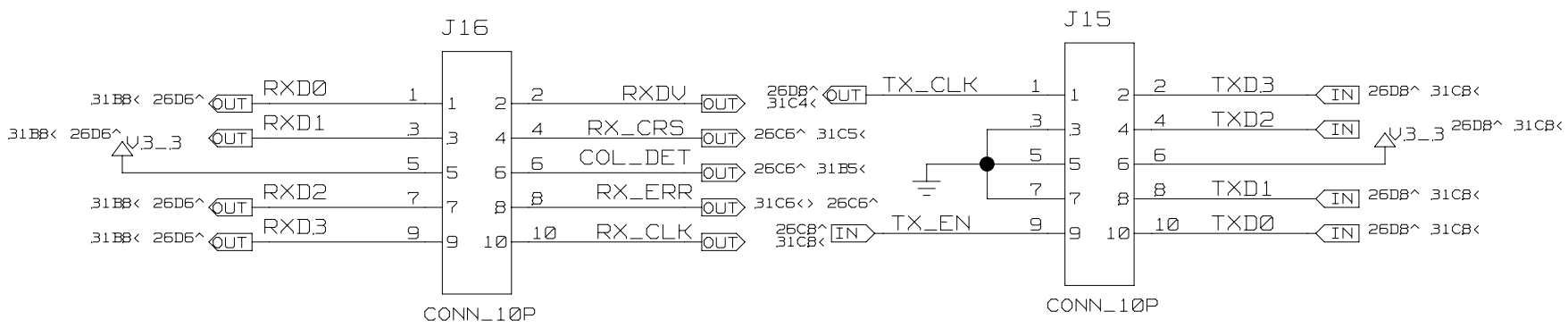


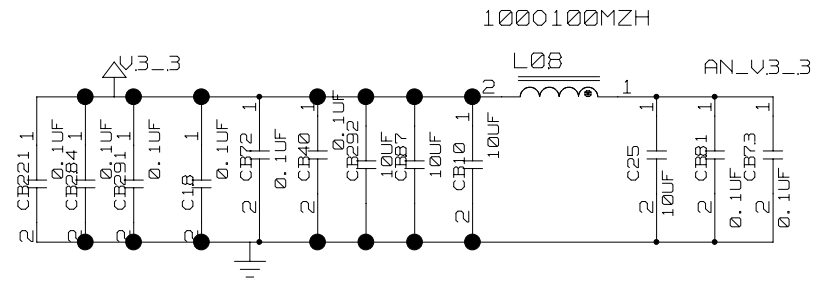
TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:8/8(BLOCK) 29/71(TOTAL)

BLOCK NAME: _z44andlan_dn. PARENT BLOCK: _z44top_dn\

CR-30 : @_ztop_lib\:_ztopdn_\(sch_1):page1_1B@_ztop_lib\:_z44top_dn\(sch_1):page1_12@_ztop_lib\:_z44anlan_dn\(sch_1):page5_154@_ztop_lib\:_mii_wan_dn\(sch_1):Page1







PLACEMENT NOTE:
TESTPOINTS (SHOWN ABOVE) MUST BE PLACED THE SAME FOR EACH PORT TO
ALLOW USE OF A DIFFERENT PHY CARD IF DESIRED. PLACEMENT SHOULD ALLOW
0.2 BETWEEN CONNECTORS.

ON Z44 CARD ALL 4 PORTS MUST BE PLACED WITH EQUAL SPACING AND A COMMON CENTER LINE

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 1/2(BLOCK) 30/71(TOTAL)

BLOCK NAME: _mii_wan_dn. PARENT BLOCK: _z44anlan_dn\

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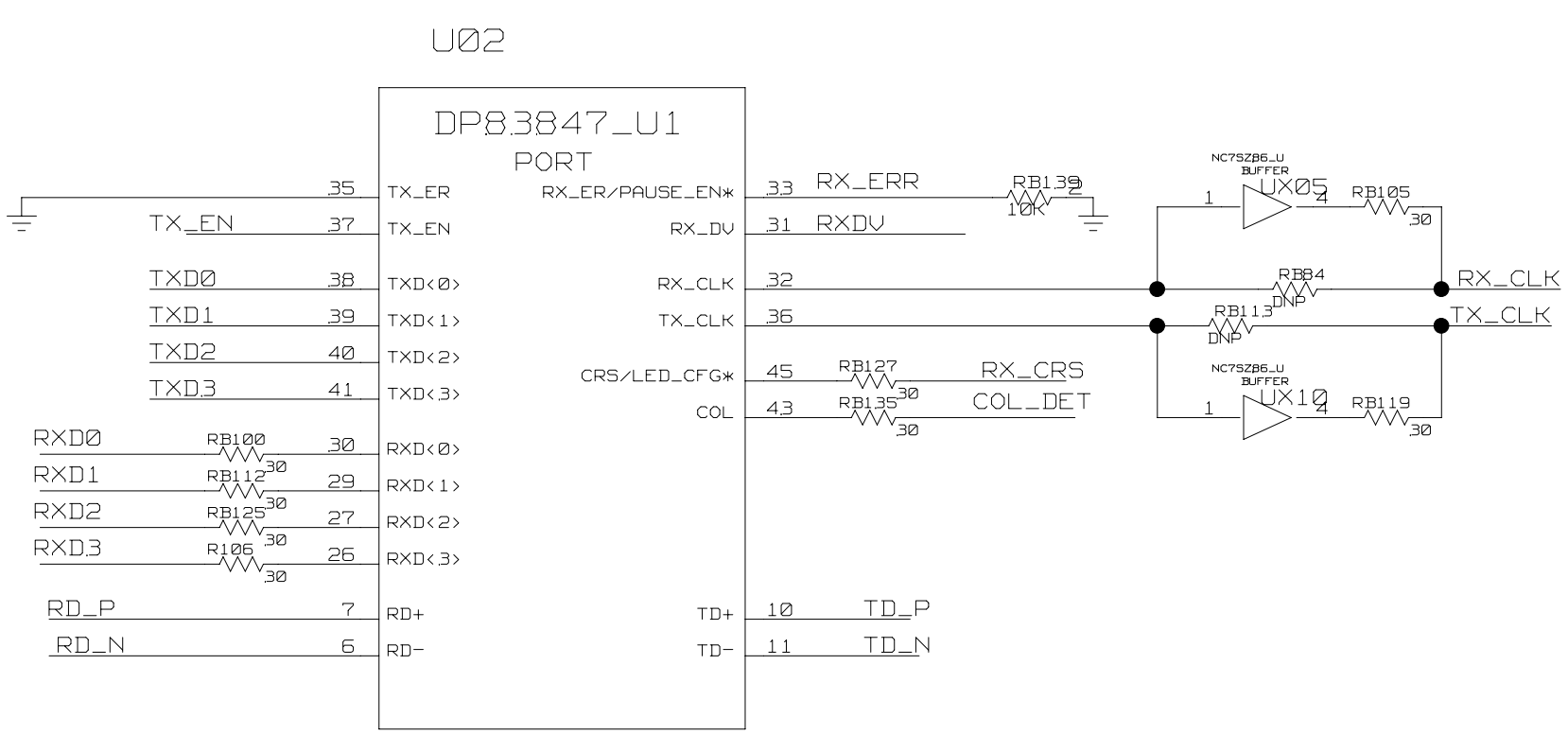
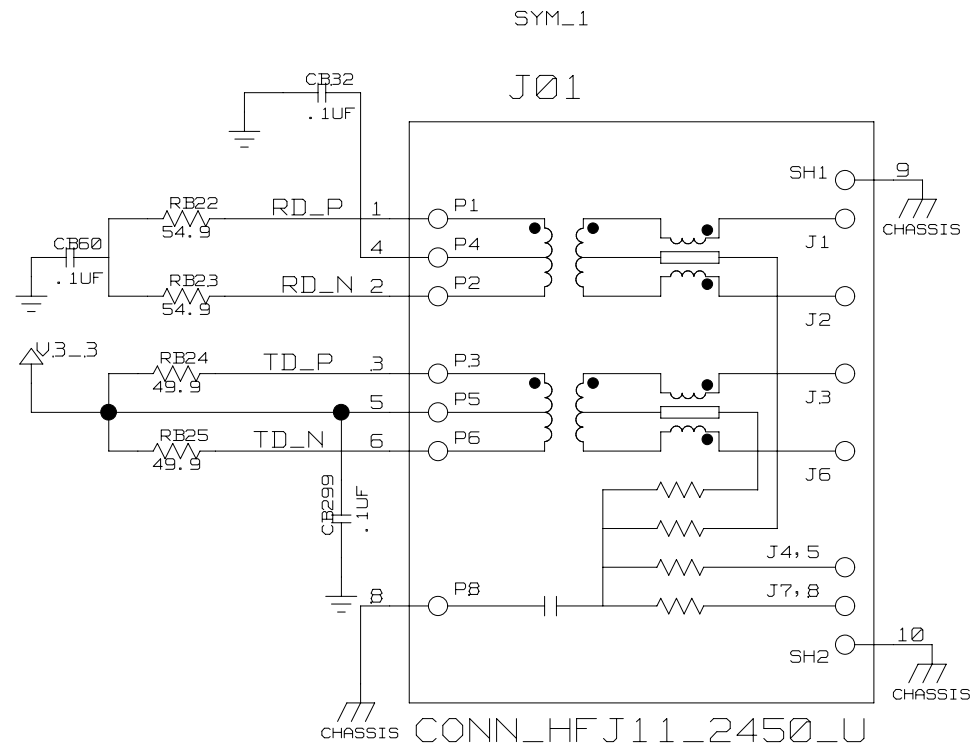




CAPS FOR XFRM CENTER TAP
SHOULD BE PLACED CLOSE TO XFRM

RESISTORS FOR TD+-/RD+-
SHOULD BE PLACED CLOSE TO PHY

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 2/2 (BLOCK) 31/71 (TOTAL)

CR-32 : @_ztop_lib\:_ztopdn_\(sch_1):page1_1B@_ztop_lib\:_z44top_dn\(sch_1):page1_12@_ztop_lib\:_z44anlan_dn\(sch_1):page5_191@_ztop_lib\:_mii_wan_dn\(sch_1):Page1

COMPONETS FOR
C1 AND RBIAS MUST
BE PLACED CLOSE TO PIN

C1PIN

C37 10UF
C103 0.1UF

R05 10.0K RBIAS

26C3^ MII_CLK
26C3^ RESET_B

U05
DP83847_U1
CONTROL

RESERVED2
RESERVED1
C1
RBIAS
X1
RESET*
X2
RESERVED10
RESERVED11
RESERVED12
RESERVED13
RESERVED14
RESERVED15
RESERVED16
RESERVED17
RESERVED18

RESERVED3
RESERVED4
RESERVED5
RESERVED6
RESERVED7
RESERVED8
RESERVED9
VDD/IO_VDD1
VDD/IO_VDD2
VDD/ANA_VDD
VDD1
VDD2
VDD3
GND1
GND2
GND3
GND4
GND5

AN_V3_3
V3_3

MDC 25 R117 30 MDC IN 26C3^
MDIO 24 MDIO IO
LED_DPLX/PHYAD0 23 LED_DPLX_ADD0 IO
LED_COL/PHYAD1 22 LED_COL_ADD1 IO
LED_GDLNK/PHYAD2 21 LED_GDLINK_ADD2 IO
LED_TX/PHYAD3 20 LED_TX_ADD3 IO
LED_RX/PHYAD4 19 LED_RX_ADD4 IO
LED_SPEED 18 TP04
AN_EN 17 RB38 5.1K AN_EN
AN_1 16 RB31 5.1K AN1
AN_0 15 RB16 5.1K AN0

LEDS NEED TO BE ATTACHED
OUTSIDE OF MODULE DUE TO
STRAP ADAPTING OPTION OF DP83847

V3_3
JP03 JP05 JP11

J20
CONN_10P

3,3B8< 26D2^ RXD0 1 2 RXDV
3,3B8< 26D2^ RXD1 3 4 RX_CRS
V3_3 5 6 COL_DET
3,3B8< 26D2^ RXD2 7 8 RX_ERR
3,3B8< 26D2^ RXD3 9 9 10 RX_CLK

J19
CONN_10P

26D4^ 3,3C4< TX_CLK 1 2 TXD3 IN 26D4^ 3,3C8<
3 4 TXD2 IN 26D4^ 3,3C8<
V3_3 5 6 26D4^ 3,3C8<
7 8 TXD1 IN 26D4^ 3,3C8<
26C4^ 3,3C8< TX_EN 9 9 10 TXD0 IN 26D4^ 3,3C8<

1000100MZH

V3_3
L06
AN_V3_3

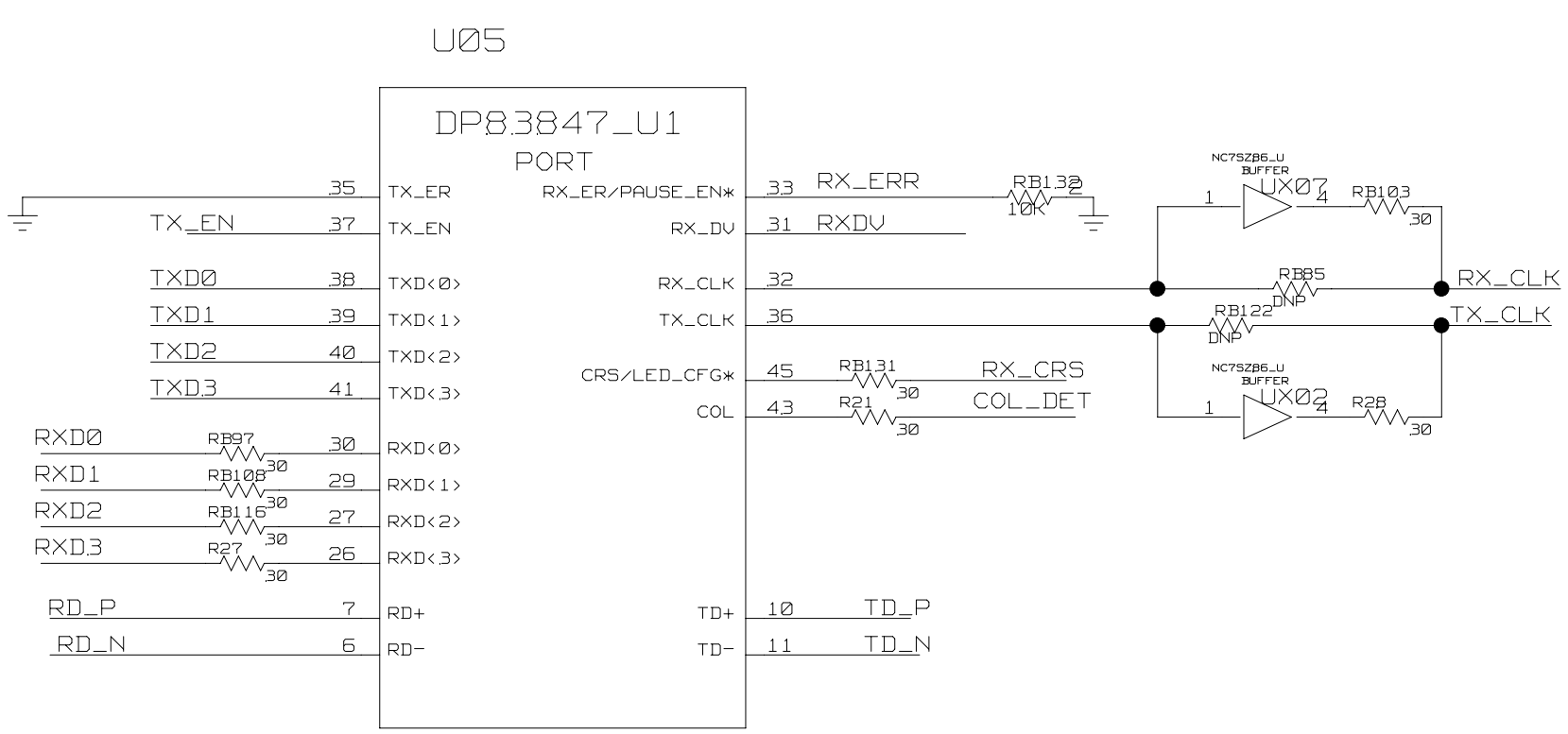
C209 0.1UF
C91 0.1UF
C88 0.1UF
C209 0.1UF
C473 0.1UF
C475 0.1UF
C174 10UF
C125 10UF
C496 10UF
C13 10UF
C146 0.1UF
C57 0.1UF

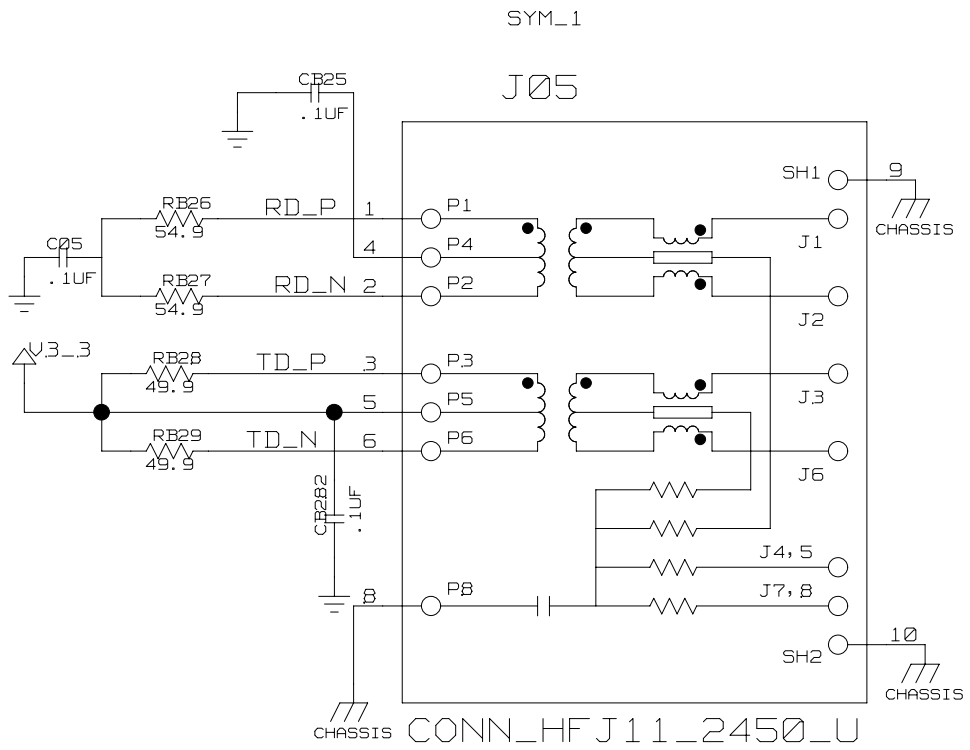
PLACEMENT NOTE:
TESTPOINTS (SHOWN ABOVE) MUST BE PLACED THE SAME FOR EACH PORT TO
ALLOW USE OF A DIFFERENT PHY CARD IF DESIRED. PLACEMENT SHOULD ALLOW
0.2 BETWEEN CONNECTORS.

ON Z44 CARD ALL 4 PORTS MUST BE PLACED WITH EQUAL SPACING AND A COMMON CENTER LINE

TITLE: DS3.3Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 1/2(BLOCK) 32/71(TOTAL)

CR-33 : @_ztop_lib\._ztopdn_\(sch_1):page1_18@_ztop_lib\._z44top_dn\(sch_1):page1_12@_ztop_lib\._z44andlan_dn\(sch_1):page5_191@_ztop_lib\._mii_wan_dn\(sch_1):Page2





CAPS FOR XFRM CENTER TAP
SHOULD BE PLACED CLOSE TO XFRM

RESISTORS FOR TD+-/RD+-
SHOULD BE PLACED CLOSE TO PHY

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 2/2 (BLOCK) 33/71 (TOTAL)

BLOCK NAME: _mii_wan_dn. PARENT BLOCK: _z44andlan_dn\

COMPONETS FOR
C1 AND RBIAS MUST
BE PLACED CLOSE TO PIN

C1PIN

C35 2 1 10UF
CB101 2 1 0.1UF

R09 10.0K RBIAS

27C3^ IN MII_CLK
27C3^ IN RESET_B

U06
DP83847_U1
CONTROL

AN_V3_3
V3_3

RESERVED3 4
RESERVED4 5
RESERVED5 8
RESERVED6 9
RESERVED7 12
RESERVED8 13
RESERVED9 34
VDD/IO_VDD1 28
VDD/IO_VDD2 56
VDD/ANA_VDD 14
VDD1 57
VDD2 59
VDD3 63

2 RESERVED2
1 RESERVED1
42 C1
RBIAS 3
X1 49
RESET* 46
48 X2
44 RESERVED10
47 RESERVED11

MDC 25 R102 30 MDC IN 27C3^
MDIO 24 MDIO IO
LED_DPLX/PHYAD0 23 LED_DPLX_ADD0 IO
LED_COL/PHYAD1 22 LED_COL_ADD1 IO
LED_GDLNK/PHYAD2 21 LED_GDLINK_ADD2 IO
LED_TX/PHYAD3 20 LED_TX_ADD3 IO
LED_RX/PHYAD4 19 LED_RX_ADD4 IO
LED_SPEED 18 TP01
AN_EN 17 RB41 5.1K AN_EN
AN_1 16 RB35 5.1K AN1
AN_0 15 RB17 5.1K AN0

LEDS NEED TO BE ATTACHED
OUTSIDE OF MODULE DUE TO
STRAP ADAPTING OPTION OF DP83847

RESERVED12 50
RESERVED13 51
RESERVED14 52
RESERVED15 53
RESERVED16 54
RESERVED17 55
RESERVED18 61
GND1 58
GND2 60
GND3 62
GND4 64
GND5 65

V3_3
JP04 JP08 JP13

J22

RXD0 1 2 RXDV
RXD1 3 4 RX_CRS
5 6 COL_DET
RXD2 7 8 RX_ERR
RXD3 9 10 RX_CLK

CONN_10P

J21

TX_CLK 1 2 TXD3
3 4 TXD2
5 6
7 8 TXD1
TX_EN 9 10 TXD0

CONN_10P

1000100MZH

V3_3
L05
AN_V3_3

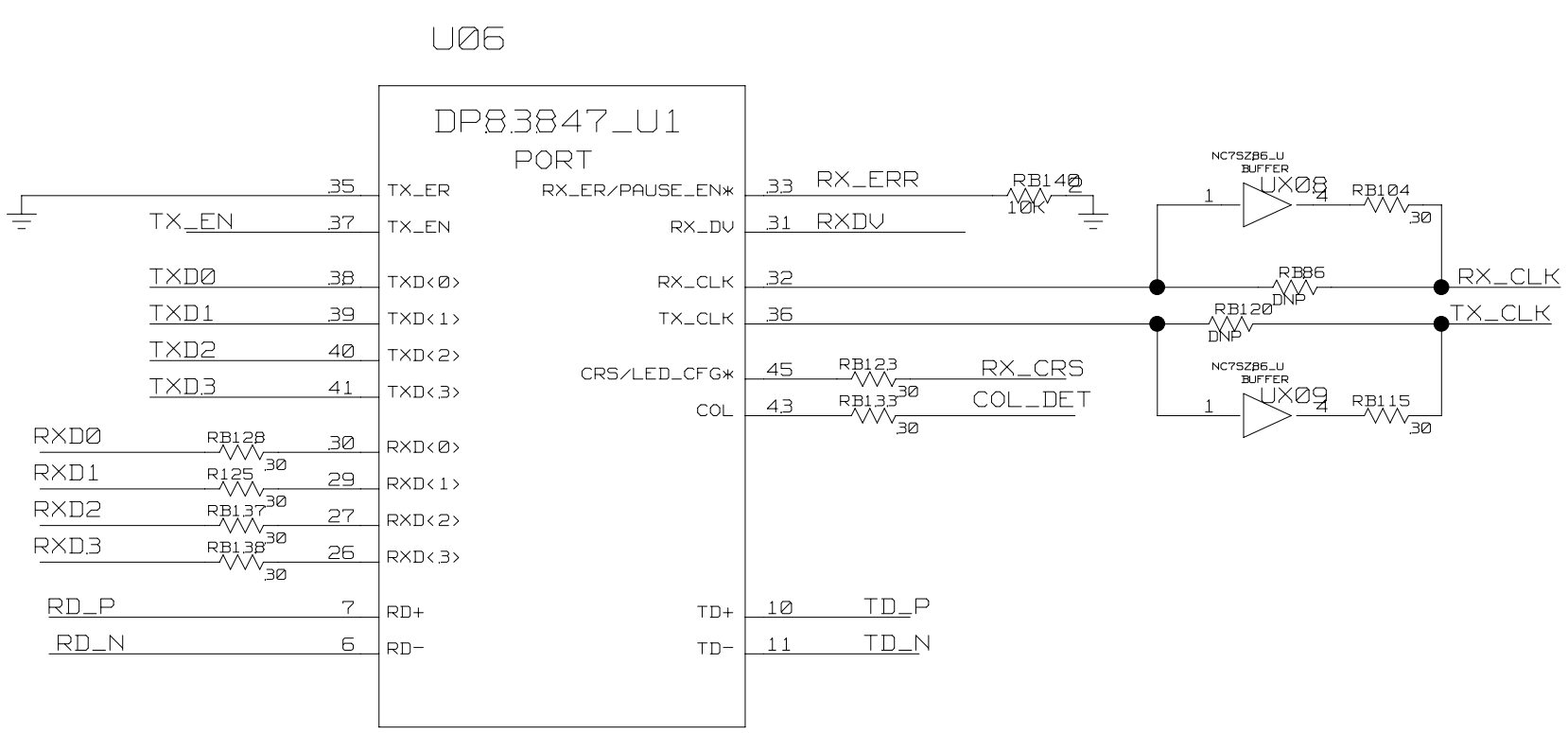
CB167 CB71 CB174 CB174 CB196 CB283 CB357 CB364 CB128 C11 CB38 CB51 0.1UF 10UF

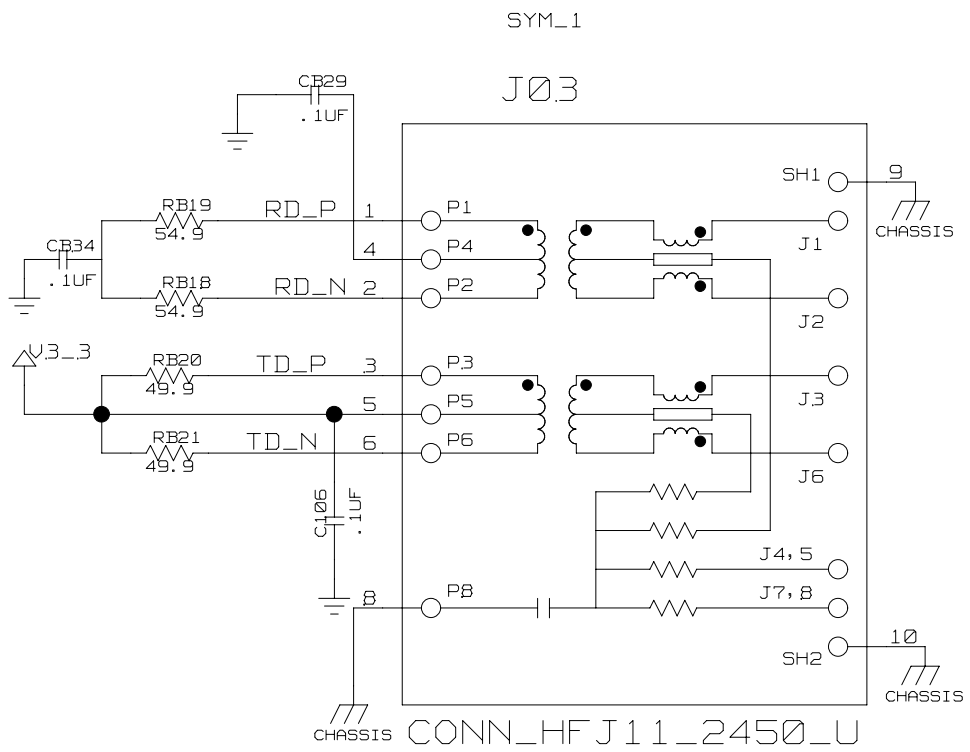
PLACEMENT NOTE:
TESTPOINTS (SHOWN ABOVE) MUST BE PLACED THE SAME FOR EACH PORT TO
ALLOW USE OF A DIFFERENT PHY CARD IF DESIRED. PLACEMENT SHOULD ALLOW
0.2 BETWEEN CONNECTORS.

ON Z44 CARD ALL 4 PORTS MUST BE PLACED WITH EQUAL SPACING AND A COMMON CENTER LINE

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 1/2(BLOCK) 34/71(TOTAL)

CR-35 : @_ztop_lib\._ztopdn_\(sch_1):page1_18@_ztop_lib\._z44top_dn\(sch_1):page1_12@_ztop_lib\._z44andlan_dn\(sch_1):page6_11@_ztop_lib\._mii_wan_dn\(sch_1):Page2





CAPS FOR XFRM CENTER TAP
SHOULD BE PLACED CLOSE TO XFRM

RESISTORS FOR TD+-/RD+-
SHOULD BE PLACED CLOSE TO PHY

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 2/2 (BLOCK) 35/71 (TOTAL)

BLOCK NAME: _mii_wan_dn, PARENT BLOCK: _z44andlan_dn\

CR-36 : @_ztop_lib\:_ztopdn_\(sch_1):page1_1B@_ztop_lib\:_z44top_dn\(sch_1):page1_12@_ztop_lib\:_z44anlan_dn\(sch_1):page6_134@_ztop_lib\:_mii_wan_dn\(sch_1):Page1

COMPONETS FOR
C1 AND RBIAS MUST
BE PLACED CLOSE TO PIN

C1PIN

C34 2 1 10UF
C28 2 1 0.1UF

R11 10.0K RBIAS

27C6^ IN MII_CLK
27C7^ IN RESET_B

U03
DP83847_U1
CONTROL

RESERVED2
RESERVED1
C1
RBIAS
X1
RESET*
X2
RESERVED10
RESERVED11
RESERVED12
RESERVED13
RESERVED14
RESERVED15
RESERVED16
RESERVED17
RESERVED18
RESERVED3
RESERVED4
RESERVED5
RESERVED6
RESERVED7
RESERVED8
RESERVED9
VDD/IO_VDD1
VDD/IO_VDD2
VDD/ANA_VDD
VDD1
VDD2
VDD3
GND1
GND2
GND3
GND4
GND5

AN_V3_3
V3_3

MDC 25 R26 30 MDC IN 27C6^
MDIO 24 MDIO IO
LED_DPLX/PHYAD0 23 LED_DPLX_ADD0 IO
LED_COL/PHYAD1 22 LED_COL_ADD1 IO
LED_GDLNK/PHYAD2 21 LED_GDLINK_ADD2 IO
LED_TX/PHYAD3 20 LED_TX_ADD3 IO
LED_RX/PHYAD4 19 LED_RX_ADD4 IO
LED_SPEED 18 TP05
AN_EN 17 RB01 5.1K AN_EN
AN_1 16 RB03 5.1K AN1
AN_0 15 RB50 5.1K AN0

LEDS NEED TO BE ATTACHED
OUTSIDE OF MODULE DUE TO
STRAP ADAPTING OPTION OF DP83847

V3_3
JP02 JP05 JP10

J18

RXD0 RXD1 RXD2 RXD3 RXDV RX_CRS COL_DET RX_ERR RX_CLK
CONN_10P

J17

TX_CLK TX_EN TXD3 TXD2 TXD1 TXD0
CONN_10P

PLACEMENT NOTE:
TESTPOINTS (SHOWN ABOVE) MUST BE PLACED THE SAME FOR EACH PORT TO
ALLOW USE OF A DIFFERENT PHY CARD IF DESIRED. PLACEMENT SHOULD ALLOW
0.2 BETWEEN CONNECTORS.

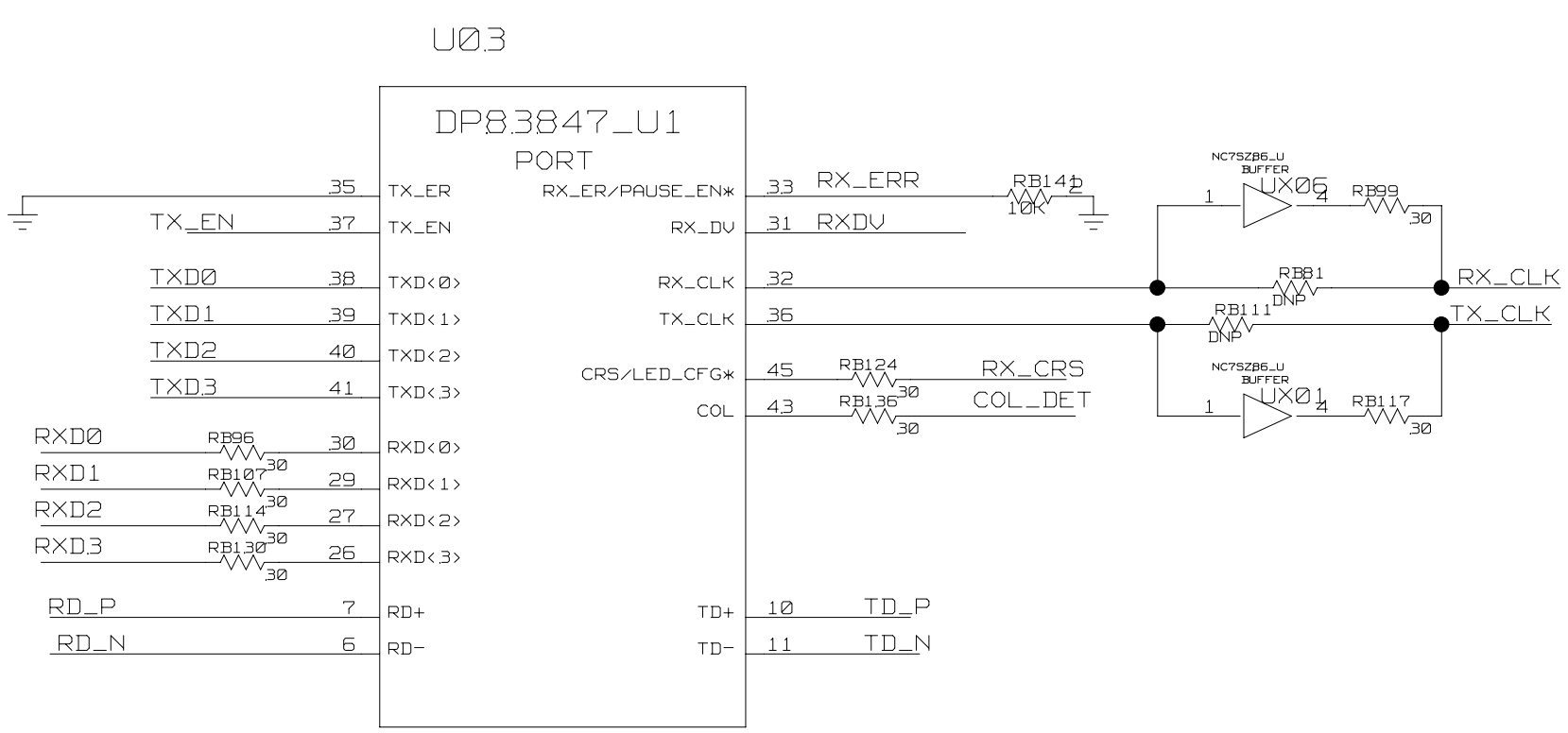
ON Z44 CARD ALL 4 PORTS MUST BE PLACED WITH EQUAL SPACING AND A COMMON CENTER LINE

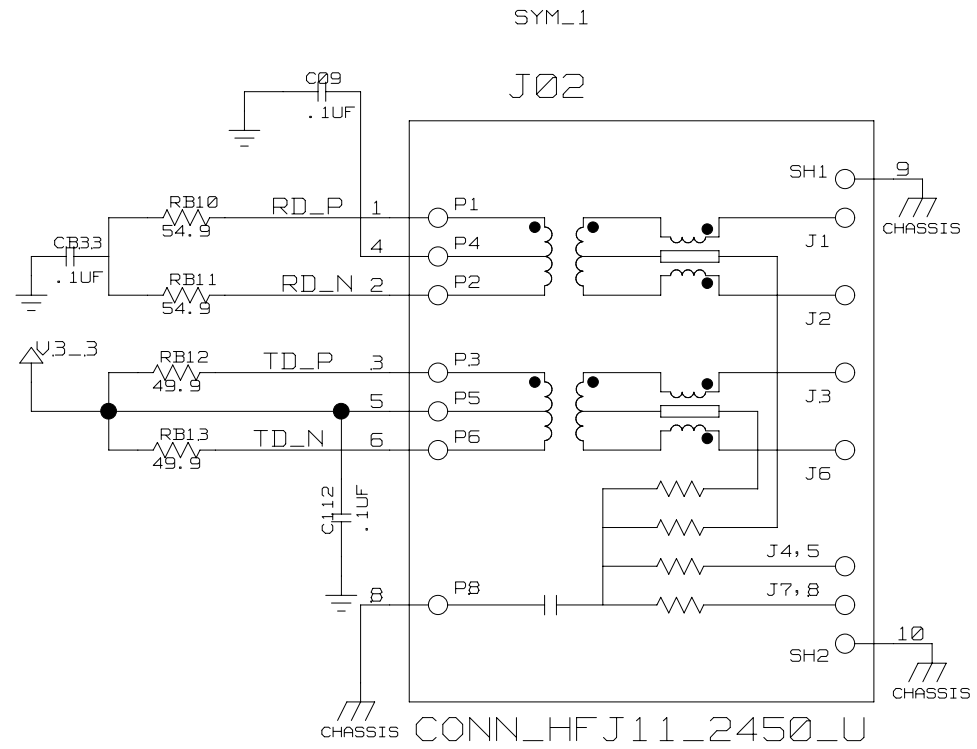
1000100MZH
L07
AN_V3_3

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 1/2(BLOCK) 36/71(TOTAL)

BLOCK NAME: _mii_wan_dn. PARENT BLOCK: _z44anlan_dn\

PRINTED Fri Oct 20 11:07:00 2006





CAPS FOR XFRM CENTER TAP
SHOULD BE PLACED CLOSE TO XFRM

RESISTORS FOR TD+-/RD+-
SHOULD BE PLACED CLOSE TO PHY

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 2/2 (BLOCK) 37/71 (TOTAL)

TQFP
NZA
MMC2107
I69

U19

88 TIM_16H_8L
96 EB3
98 EB2
100 EB1
101 EB0
104 PQB3
105 PQB2
106 PQB1
107 PQB0
108 PQA4
109 PQA3
110 PQA1
111 PQA0
133 ONCE_TDI
135 2107_TDO

INT6* EB3* EB2* EB1* EB0* PQB3 PQB2 PQB1 PQB0 PQA4 PQA3 PQA1 PQA0 TDI TDO

ICOC23 52 ICOC23
ICOC22 53 ICOC22
ICOC21 54 ICOC21
ICOC20 55 ICOC20
ICOC13 56 ICOC13
ICOC12 57 ICOC12
ICOC11 58 ICOC11
ICOC10 61 ICOC10
I68
GND TEST 63 TEST
SCI2_OUT 66 TXD2
SCI2_IN 68 RXD2
SCI1_OUT 69 TXD1
SCI1_IN 70 RXD1

MMC2107
CONTROL

CSE1 60 CSE1
CSE0 62 CSE0
TC2 67 TC2
TC1 78 TC1
CS3* 81 CS3
CS2* 83 CS2
CS1* 85 CS1
CS0* 86 CS0
RESET* 118 RESET_B
CLKOUT 128 CPUCLK_OUT
RSTOUT* 120 PROC_RESET_OUT
SCK 93 SCK
DE* 143 ONCE_DE_B
SS* 94 SS

INT7* INT5* INT4 INT3* INT2* INT1* INT0* YC0 MOSI MISO XTAL EXTAL TCLK TRST* TMS

89 USER_LED1
84 USER_LED2
82 INT3
79 INT4
75 RUN_KIT_USR
72 TIM_STATUS
71 INT2
80 YC0
90 MOSI
91 MISO
124 XTAL
125 OSC_MCU
130 ONCE_TCLK
142 ONCE_TRST_B
138 ONCE_TMS

SOT143
2.93V
MAX811SEUS-T
I70
UB01

I64
SW07

MAX811_U
MR*
GND
VCC
RESET*
V3_3
RESET_B

TQFP
NZA
MMC2107
I51
U19

59 RW
95 OE*
97 RCON
99 TA*
102 TEA*
92 VSTBY
113 VRH
112 VRL
87 VPP
115 VDDA
74 VDDF
103 VDDH
123 VDDSYN
141 VDD8
129 VDD7
77 VDD6
65 VDD5
45 VDD4
33 VDD3
19 VDD2
9 VDD1

RW OE* RCON TA* TEA* VRH FLASH_VPP

VDDSYN
RB159 2 0.0 1
C87 2 .1UF 1
V3_3

MMC2107
PORT

31 144 D31
30 1 D30
29 2 D29
28 3 D28
27 4 D27
26 5 D26
25 7 D25
24 10 D24
23 12 D23
22 15 D22
21 16 D21
20 17 D20
19 20 D19
18 21 D18
17 22 D17
16 25 D16
15 27 D15
14 30 D14
13 31 D13
12 34 D12
11 35 D11

A22 116 22
A21 117 21
A20 119 20
A19 121 19
A18 122 18
A17 131 17
A16 132 16
A15 134 15
A14 136 14
A13 137 13
A12 139 12
A11 6 11
A10 11 10
A9 13 9
A8 14 8
A7 23 7
A6 24 6
A5 26 5
A4 28 4
A3 29 3
A2 47 2
A1 49 1
A0 50 0

PA<22..0>

D10 36 10
D9 37 9
D8 38 8
D7 39 7
D6 40 6
D5 41 5
D4 42 4
D3 43 3
D2 45 2
D1 48 1
D0 51 0

PD<31..0>

VSSA 114
VSSF 73
VSSSYN 126
VSS8 140
VSS7 127
VSS6 76
VSS5 64
VSS4 44
VSS3 32
VSS2 18
VSS1 8

MMC2107
PROCESSOR RESOURCE CARD

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 1/7 (BLOCK) 38/71 (TOTAL)

RESET CONFIGURATION

MASTER MODE

FULL DRIVE

XTAL W/ PLL

INTERNAL
FLASH ENABLE

BOOT
INTERN/EXTERN

R93 10K — PD<26> — V3_3
RB300 10K — PD<17>
RB238 10K — PD<16>
RB301 10K — PD<21>
RB263 10K — PD<23>
R92 10K — PD<22>
R127 10K — PD<28>

RCON — R153 10K

RB264 10K — PD<19>
RB237 10K — PD<18>

WHEN SET FOR
BOOT INTERNAL
D18 HAS A 10K LOAD TO GND
BOOT EXT
D18 HAS A 10.5K LOAD TO V.3V

V3_3
R250 1.0K, R251 1.0K, RB143 1.0K, RB152 1.0K, R244 1.0K, RB150 1.0K, RB147 1.0K
V5_0
I69 SW22 SWITCH 8 POS
BTS_0BSXI
BIS10BSXI
BIS00BSXI
INT3
INT4
USERFPGA2
INT5
RB126 1.0K — V3_3
FLASH_VPP — RB118 30 — DS17 I65 AMBER — V3_3
0L_SMT0805_10PCT
ECJ-2VB1C104K
CB149 .1UF

V3_3
CY62128V
ZA I54 UB0
FB0, OE, CS0
VCC, N_C, WE*, OE*, CE2, CE1*, GND
A16 5, A15 2, A14 25, A13 3, A12 26, A11 4, A10 28, A9 27, A8 31
A7 6, A6 7, A5 8, A4 9, A3 10, A2 11, A1 12, A0 23
IO7 31, IO6 30, IO5 29, IO4 28, IO3 27, IO2 26, IO1 25, IO0 24
PD<31..24>
PA<17..1>

V3_3
CY62128V
ZA I18 U14
FB1, OE, CS0
VCC, N_C, WE*, OE*, CE2, CE1*, GND
A16 9, A15 12, A14 25, A13 11, A12 26, A11 10, A10 28, A9 27, A8 31
A7 8, A6 7, A5 6, A4 5, A3 4, A2 3, A1 2, A0 23
IO7 23, IO6 22, IO5 21, IO4 20, IO3 19, IO2 18, IO1 17, IO0 16
PD<23..16>
PA<17..1>

RESET AND CHIP CONFIGURATION

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 2/7 (BLOCK) 39/71 (TOTAL)

BLOCK NAME: _motprocrescard_dn. PARENT BLOCK: _z44top_dn\

X02
I47
8.0MHZ
OSC_MCU
R90
1.0M
PLACE PADS FOR CAP
BUT DO NOT POPULATE
XTAL

V3_3
R102 10K
R11B 10K
J41
CON14P
CON14P
NAD
I1
CON14P
ONCE_TDI
2107_TDO
ONCE_TCLK
RESET_B
ALIGN KEY
ONCE_TMS
ONCE_DE_B
ONCE_TRST_B
R91 10K
I11

V5_0
C43 1UF
C47 10UF
CB114
C39 1UF
R78 330
C35 68UF
U09
MAX1675
OUT
LX
GND
SHDN
FB
LBI
LBO*
REF
CB148 .1UF
I13
L09 22.0UH
C104 68UF

MAX3233E
MAX3233E
NAD
I31
UB07
MAX3233E
R2OUT
INVALID*
T2IN
T1IN
FORCEON
R1OUT
T1OUT
R1IN
VCC
FORCEOFF*
R2IN
T2OUT
GND
V-
C2-
C2+
C1-
C1+
V+2
V+1
SCI1_OUT
SCI1_IN
PRT1_OUT
PRT1_IN

SMT1206_5PCT
ERJ-8GEYJ5R6V
R107 5.6
C118 1UF
C91 1UF
CB3 1UF
CB4 1UF
CB35 1UF
CB262 1UF
CB466 1UF
CB484 1UF
CB199 1UF
VDDSYN

RB287 10K
RB286 10K
RB200 10K
I35
J36
PRT1_OUT
PRT1_IN
CONN_DB9P

JTAG CONFIGURATION
ONCETDI PIN
MMC2107
ONCETDO PIN
TDI
...FPGA+FLASH...

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 3/7 (BLOCK) 40/71 (TOTAL)

CR-41 : @_ztop_lib\:_ztopdn_\(sch_1):page1_1B@_ztop_lib\:_z44top_dn\(sch_1):page2_1I@_ztop_lib\:_motprocrescard_dn\(sch_1):Page4

J25

CONN_10P

SPARE_B<5..0>

BANK 1

BANK 0

BANK 2

BANK 3

U16

XC2S50_BGA

PA<16..0>

PD<31..16>

X_INIT

TIM_INTERUPT_IND

TIM_INTERUPT

USER_LED1

USER_LED2

PROC_RESET_OUT

CFG_DIN

RB193 330

R194 330

R195 330

RB145 330

DS27 RED

DS37 RED

DS40 RED

DS19 GREEN

V3_3

RED

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:4/7(BLOCK) 41/71(TOTAL)

BLOCK NAME: _motprocrescard_dn. PARENT BLOCK: _z44top_dn\

I34
CONN_THRU-HOLE
NOPOP
NOADD

J26
CONN_10P

SPARE_A<10..1>

D_DUT<7..0>

CPUCLK_OUT

BANK 5

I46
U16
XC2S50_BGA

BANK 4

BANK 6

BANK 7

XA<11..0>

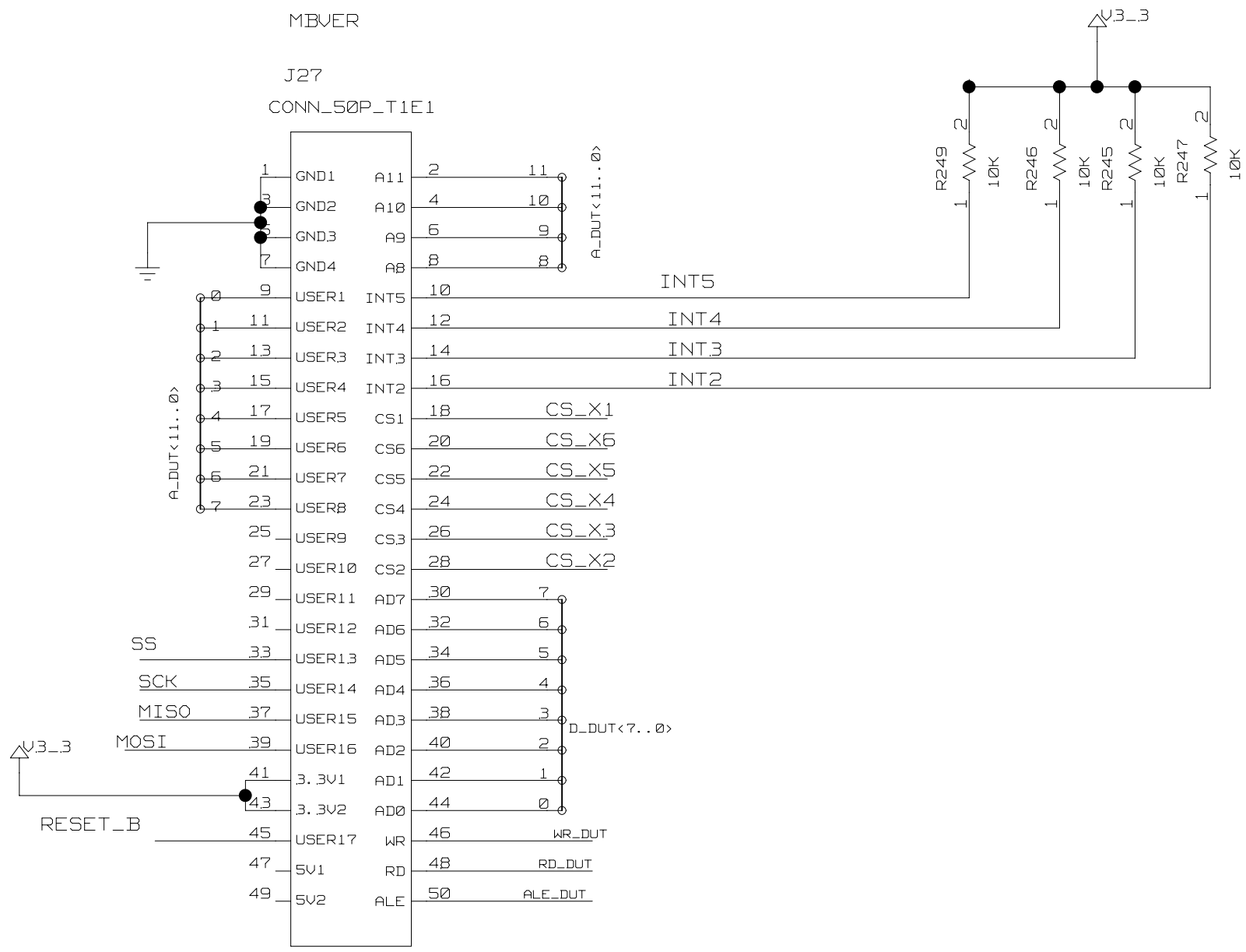
XD<7..0>

A_DUT<11..0>

BUS MODE
DETECTION (DUT AT CS_X2)

WE ALSO FUNCTIONS AS ALT_WR_RW
RW ALSO FUNCTIONS AS ALT_RD_DS

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 5/7 (BLOCK) 42/71 (TOTAL)



IN INT5 39C3<> 42A6<> 43C6<> 21C7^
IN INT4 3BA7<> 39C3<> 43C6<> 21C7^
IN INT3 3BA7<> 39D3<> 43C6<> 21C7^
IN INT2 3BA7<> 43C6<> 21C7^

RESET_B OUT 3BA4> 3BB5<> 40C3<> 21C5^ 43A7< 44B1<

IN BTS_DUT 42C3<> 21B7^
IN BIS0_DUT 42C3<> 21B7^
IN BIS1_DUT 42C3<> 21B7^

TDO_NU OUT 44A6<> 21B6^
IN TCK_NU 44A6<> 21B6^
IN TDI_NU 44A6<> 21B6^
IN TMS_NU 44A6<> 21B6^

CS_X4 OUT 42A4<> 43B6<> 21C5^
CS_X5 OUT 42A4<> 43B6<> 21C5^
CS_X1 OUT 42B3<> 43B6<> 21C5^
CS_X2 OUT 42B3<> 43B6<> 21C5^
CS_X3 OUT 42A4<> 43B6<> 21C5^
WR OUT 42B3<> 21B5^
RW_X OUT 42B3<> 21B5^
WR_DUT OUT 42C3<> 43A6<> 21B5^
RD_DUT OUT 42C3<> 43A6<> 21B7^
A_DUT<11..0> OUT 21B7^ 42A6 43B7 43C6
42B7 21B5^XA<15..0> OUT
D_DUT<7..0> IO
XD<7..0> IO

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 6/7 (BLOCK) 43/71 (TOTAL)

BLOCK NAME: _motprocrescard_dn, PARENT BLOCK: _z44top_dn\

U12

XILINX_XCF01S

UB11

MAX1792

U16

XC2S50_BGA

CONTROL

J43

CONN_10P

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 7/7 (BLOCK) 44/71 (TOTAL)

DS21458 WAN INTERFACE BLOCK

I73
2.048MHZ_3.3V

YB02
OSC
1 — 1 VCC — 8 — V3_3
4 GND OUT — 5 — RB160 30 — MCLK — 46C7<
RB184 30 — MCLK2FPGA — 53B6<>

V3_3 — P4 P5 P6 C11 C12 C13 D3 E3 F3 L14 M14 N14 H1 J16 A9 T8 R6 T6 A11 B11 F1 F2 L15 L16
DVDD11 DVDD12 DVDD13 DVDD21 DVDD22 DVDD23 DVDD31 DVDD32 DVDD33 DVDD41 DVDD42 DVDD43 RVDD1 RVDD2 RVDD3 RVDD4 TVDD11 TVDD12 TVDD21 TVDD22 TVDD31 TVDD32 TVDD41 TVDD42

V3_3 — C42 10UF, C48 10UF, CR236 10UF, CR126 10UF, CR154 10UF, C103 10UF, C115 10UF, CR340 10UF, CR112 10UF

V3_3 — CR179 1 0.1UF 2, CR144 1 0.1UF 2, CR161 1 0.1UF 2, CR160 1 0.1UF 2, CR156 1 0.1UF 2, CR120 2 0.1UF 1, CR204 1 0.1UF 2, CR138 1 0.1UF 2, CR152 2 0.1UF 1

V3_3 — CR155 2 0.1UF 1, CR127 2 0.1UF 1, CR201 1 0.1UF 2, CR210 1 0.1UF 2

U20
DS21458_U

CONTROL

K14	JTRST	
52C1< 52C8<> 52A7<> XI_TMS	J15	JTMS
52C1< 52C8<> 52A7<> ONCE_TCK	K16	JTCLK
52C6<> JTD_FLASH_TDO	C10	JTDI
52A7<> JTDO0458	K13	JTDO
55D5> 46A4<> OUT WAN_INT	H5	INT*
51D7< LIUC	D9	LIUC
46D7< MCLK	H4	MCLK1
	J12	MCLK2
	H9	RCLKI
	H10	RNEGI
	G8	RPOSI
	J14	TEST1
	J13	TEST2
46A1<> IN RESET_AH	K15	TSTRST
55A4< IN CS	M8	CS*
55A2<> 54C7<> IN RD	A10	RD*
55A3<> 54C7<> IN WR	C9	WR*
	N4	DVSS11
	N5	DVSS12
	N6	DVSS13
	D11	DVSS21
	D12	DVSS22
	D13	DVSS23

DVSS31 DVSS32 DVSS33 DVSS41 DVSS42 DVSS43 RVSS11 RVSS12 RVSS13 RVSS21 RVSS22 RVSS23 RVSS31 RVSS32 RVSS33 RVSS41 RVSS42 RVSS43 TVSS11 TVSS12 TVSS21 TVSS22 TVSS31 TVSS32 TVSS41 TVSS42 NC1 NC2 NC3
D4 E4 F4 L13 M13 N13 N1 J1 M1 E16 H16 D16 A5 A8 A4 T12 T13 T9 R5 T5 A12 B12 E1 E2 M15 M16 K9 P3 E9

I37
NA
NC7SZ86

ADDR<9..0> IN 54C7 55A5 55A7

A<0>	H2	0
A<1>	E10	1
A<2>	H3	2
A<3>	G4	3
A<4>	N7	4
A<5>	B9	5
A<6>	T7	6
A<7>/ALE_A5	G2	7
A<8>	H6	8
A<9>	J11	9

DAT<7..0> IO 54C3 55A2 55A4

AD<0>	P8	0
AD<1>	D10	1
AD<2>	N8	2
AD<3>	P7	3
AD<4>	M7	4
AD<5>	R7	5
AD<6>	G1	6
AD<7>	G3	7

BTS	B10	BTS 51C7<
MUX	R8	MUX 51B7<
ESIBRD	H8	ESIBRD 51C7<
ESIBS<0>	J8	ESIBR0 51C7<
ESIBS<1>	J9	ESIBR1 51C7<

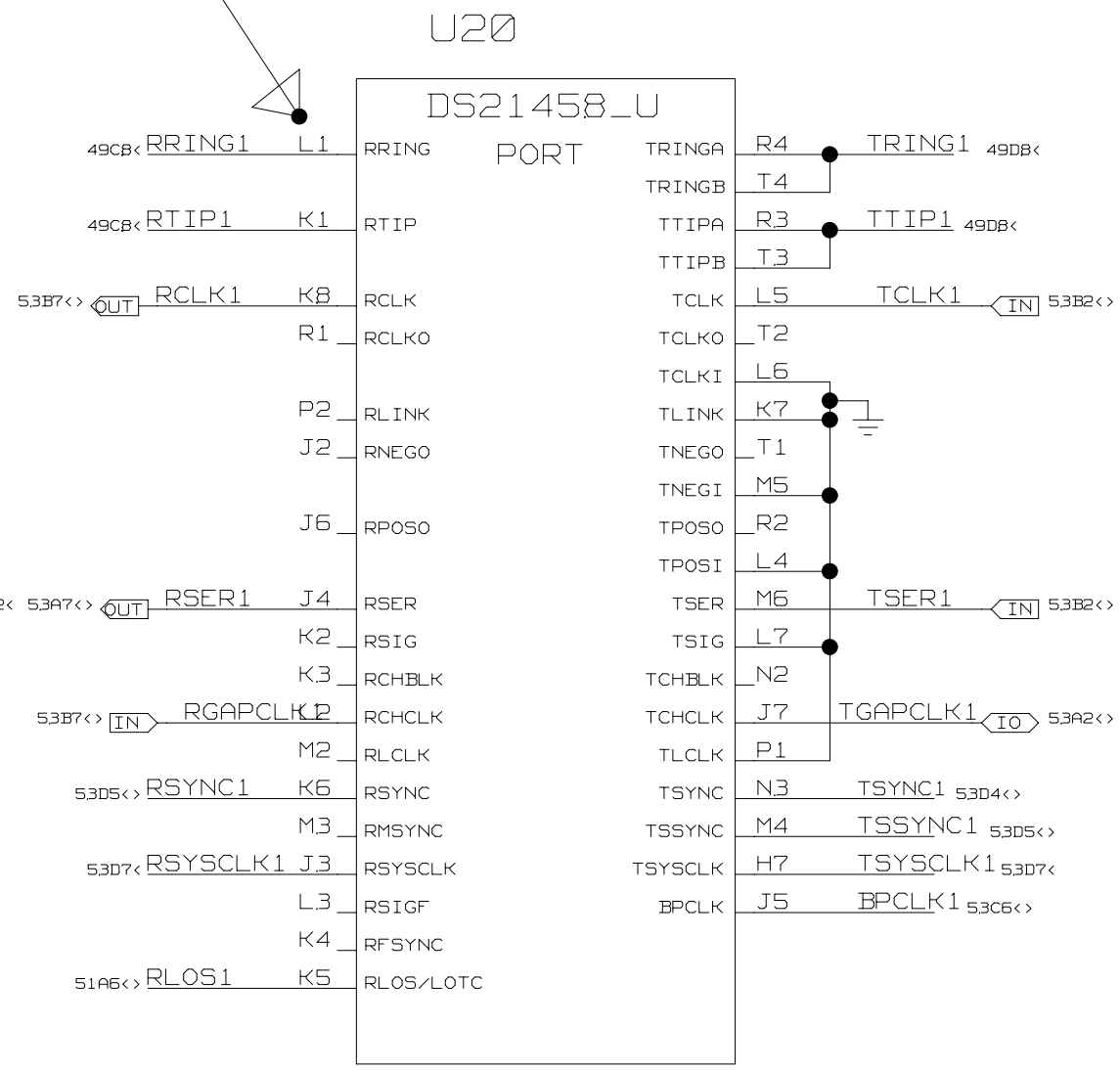
I41
NA
NC7SZ86
NC7SZB6_U
52B1< 55D6<> RESET_B — UXB05 INVERTER — RESET_AH 46B7<

V3_3 — RED DS25 — R1142 330 — NC7SZB6_U BUFFER UX11 — WAN_INT 46C7> 55D5>

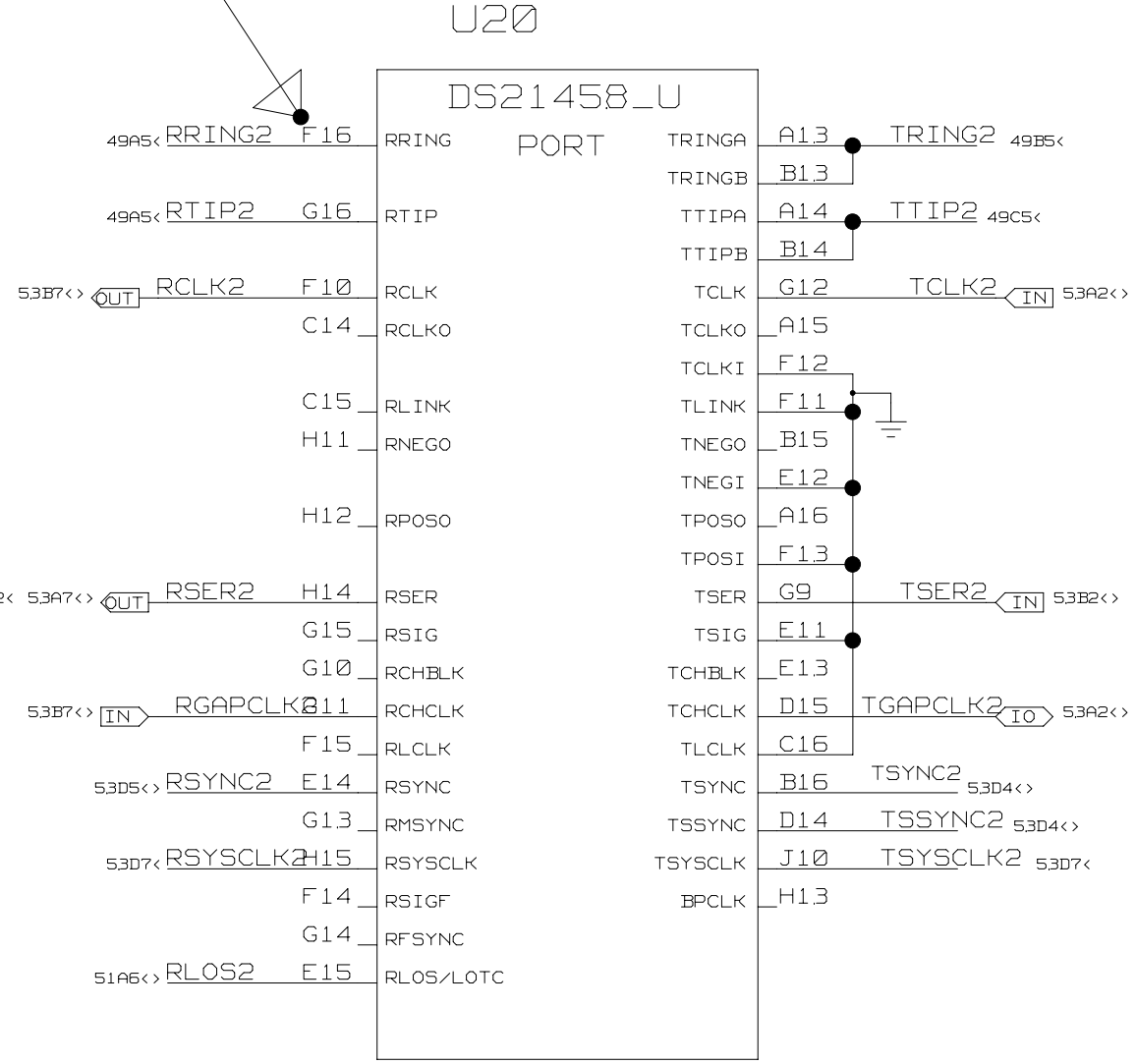
TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 46/71(TOTAL)

CR-47 : @_ZTOP_LIB\._ZTOPDN_\(SCH_1):PAGE1_T11@_ZTOP_LIB\._WAN4Z44_DN\(SCH_1):PAGE1_T1@_ZTOP_LIB\._QUADTE1WAN_DN\(SCH_1):PAGE2

PORT1_RRING = PIN L1



PORT2_RRING = PIN F16



TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 2/10 (BLOCK) 47/71 (TOTAL)

BLOCK NAME: _quadte1wan_dn. PARENT BLOCK: _wan4z44_dn\

CR-4B : @_ZTOP_LIB\._ZTOPDN_\(SCH_1):PAGE1_T11@_ZTOP_LIB\._WAN4Z44_DN\(SCH_1):PAGE1_T1@_ZTOP_LIB\._QUADTE1WAN_DN\(SCH_1):PAGE3

PORT3_RRING = PIN A6

U20

DS21458_U

PORT

50C8<	RRING3	A6	RRING	TRINGA	D1	TRING3	50D8<
				TRINGB	D2		
50C8<	RTIP3	A7	RTIP	TTIPA	C1	TTIP3	50D8<
				TTIPB	C2		
53B7<> OUT	RCLK3	G5	RCLK	TCLK	F6	TCLK3 IN	53A2<>
		A2	RCLKO	TCLKO	B2		
				TCLKI	F7		
		C3	RLINK	TLINK	G7		
		F8	RNEGO	TNEGO	A1		
				TNEGI	E5		
		F9	RPOSO	TPOSO	B1		
				TPOSI	D5		
53C2< 53A7<> OUT	RSER3	C8	RSER	TSER	G6	TSER3 IN	53B2<>
		B7	RSIG	TSIG	F5		
		C7	RCHBLK	TCHBLK	C5		
53B7<> IN	RGAPCLK3	D7	RCHCLK	TCHCLK	B4	TGAPCLK3 IO	53A2<>
		B6	RLCLK	TLCLK	C4		
53D4<>	RSYNC3	B5	RSYNC	TSYNC	B3	TSYNC3	53D4<>
		E6	RMSYNC	TSSYNC	A3	TSSYNC3	53D4<>
53D7<	RSYSCLK3	B8	RSYSCLK	TSYSCLK	D8	TSYSCLK3	53C7<
		E7	RSIGF	BPCLK	E8		
		C6	RFSYNC				
51A6<>	RLOS3	D6	RLOS/LOTC				

PORT4_RRING = PIN T11

U20

DS21458_U

PORT

50A5<	RRING4	T11	RRING	TRINGA	N15	TRING4	50B5<
				TRINGB	N16		
50A5<	RTIP4	T10	RTIP	TTIPA	P15	TTIP4	50C5<
				TTIPB	P16		
53B7<> OUT	RCLK4	K12	RCLK	TCLK	L9	TCLK4 IN	53A2<>
		P14	RCLKO	TCLKO	R16		
				TCLKI	L11		
		T15	RLINK	TLINK	L12		
		P10	RNEGO	TNEGO	T16		
				TNEGI	M12		
		N10	RPOSO	TPOSO	R15		
				TPOSI	L10		
53C2< 53A7<> OUT	RSER4	P9	RSER	TSER	K10	TSER4 IN	53B2<>
		R10	RSIG	TSIG	K11		
		R11	RCHBLK	TCHBLK	R13		
53B7<> IN	RGAPCLK4	M9	RCHCLK	TCHCLK	P13	TGAPCLK4 IO	53A2<>
		R12	RLCLK	TLCLK	T14		
53D4<>	RSYNC4	N12	RSYNC	TSYNC	R14	TSYNC4	53D4<>
		M10	RMSYNC	TSSYNC	M11	TSSYNC4	53D4<>
53D7<	RSYSCLK4	R9	RSYSCLK	TSYSCLK	L8	TSYSCLK4	53C7<
		N11	RSIGF	BPCLK	N9		
		P11	RFSYNC				
51A6<>	RLOS4	P12	RLOS/LOTC				

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:3/10(BLOCK) 48/71(TOTAL)

BLOCK NAME: _quadte1wan_dn, PARENT BLOCK: _wan4z44_dn\

CR-49 : @_ZTOP_LIB\._ZTOPDN_\(SCH_1):PAGE1_I11@_ZTOP_LIB\._WAN4Z44_DN\(SCH_1):PAGE1_I1@_ZTOP_LIB\._QUADTE1WAN_DN\(SCH_1):PAGE4

TTIP1 R2082 C176 1UF XMIT L10 I11

TRING1 R2072

I13 RJ45_4PORT JB12 RJ45

RTIP1 RB3282 RCV I14

RRING1 RB3272

RB313 2.61R RB315 2.61R

CB395 0.1UF

47C2 TTIP2 R2042 C173 1UF XMIT L10 I2

47C2 TRING2 R2032

I25 RJ45_4PORT JB12 RJ45

47C4 RTIP2 RB3222 RCV I26

47C4 RRING2 RB3212

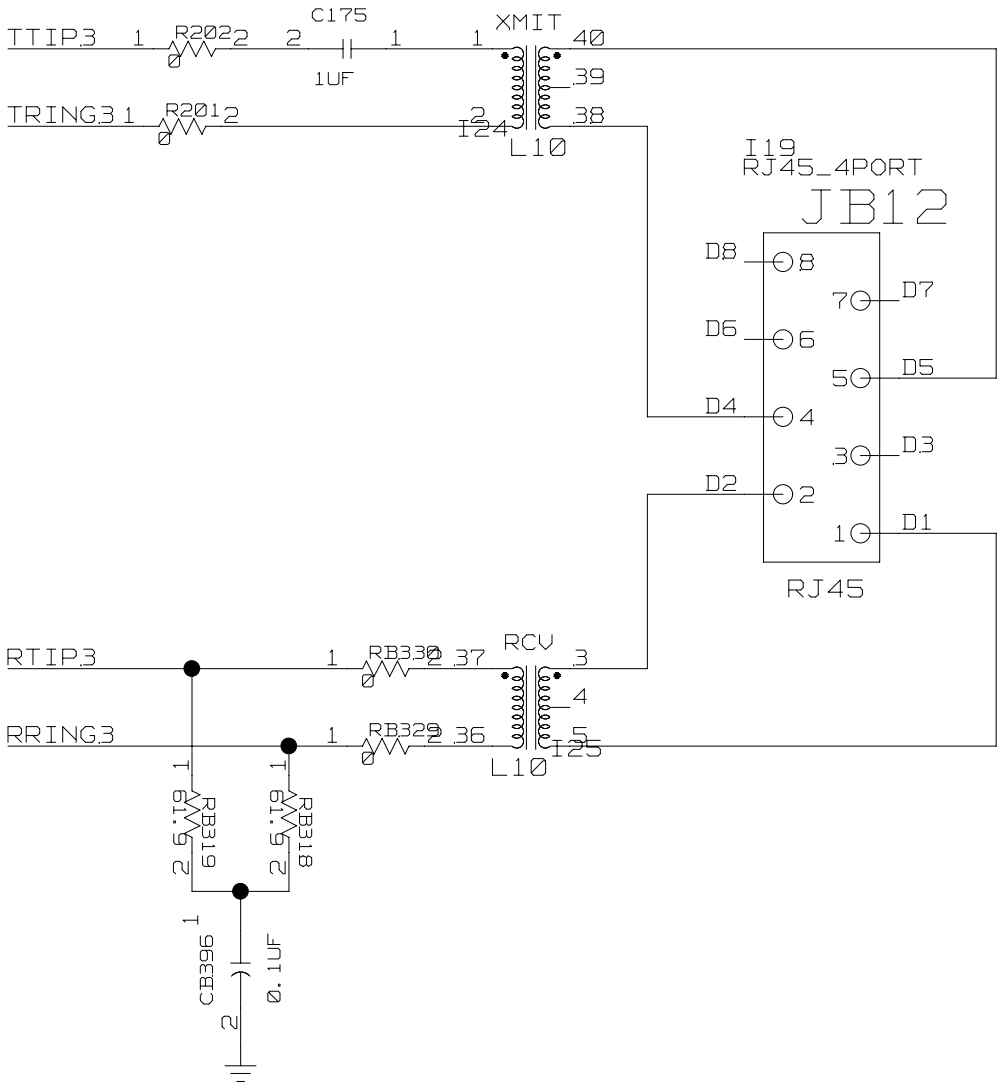
RB313 2.61R RB312 2.61R

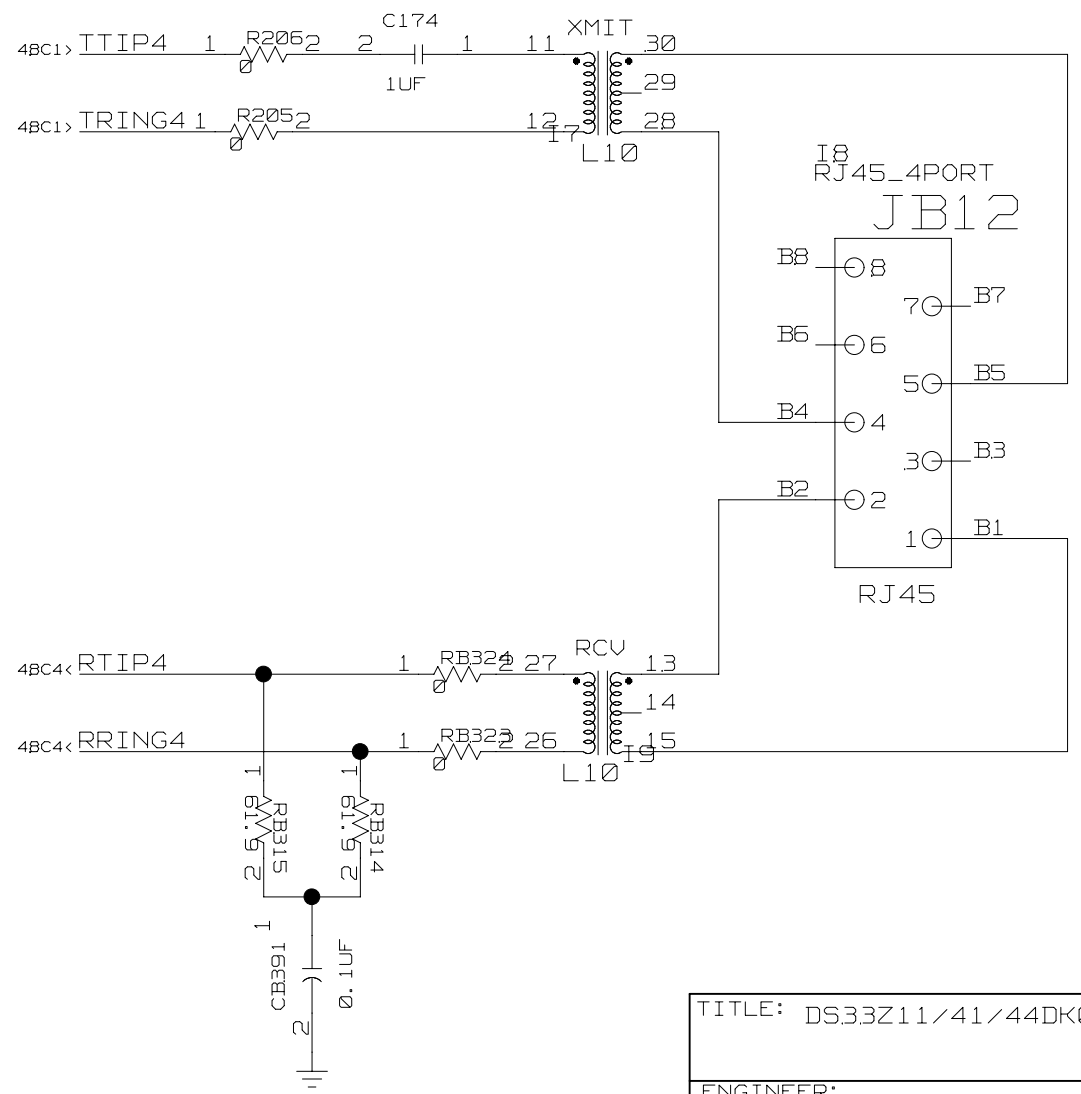
CB390 0.1UF

THE PCB LAYOUT INCORRECTLY USES PINS 38-40, 33-35, 28-30 AND 23-25
AS THE TX PRIMARY. THIS HAS BEEN CORRECTED IN THE SCHEMATIC,
THE PCB / ASSEMBLY HAS BEEN MODIFIED TO ACCOMMODATE THIS.

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:4/10(BLOCK) 49/71(TOTAL)

BLOCK NAME: _quadte1wan_dn. PARENT BLOCK: _wan4z44_dn\



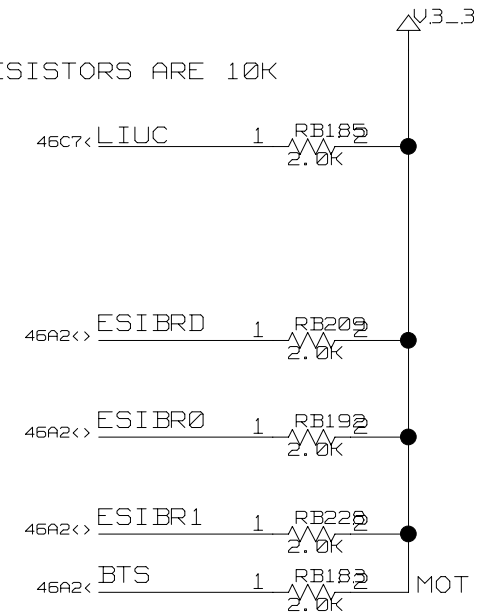


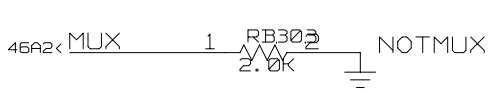
THE PCB LAYOUT INCORRECTLY USES PINS 38-40, 33-35, 28-30 AND 23-25 AS THE TX PRIMARY. THIS HAS BEEN CORRECTED IN THE SCHEMATIC, THE PCB / ASSEMBLY HAS BEEN MODIFIED TO ACCOMMODATE THIS.

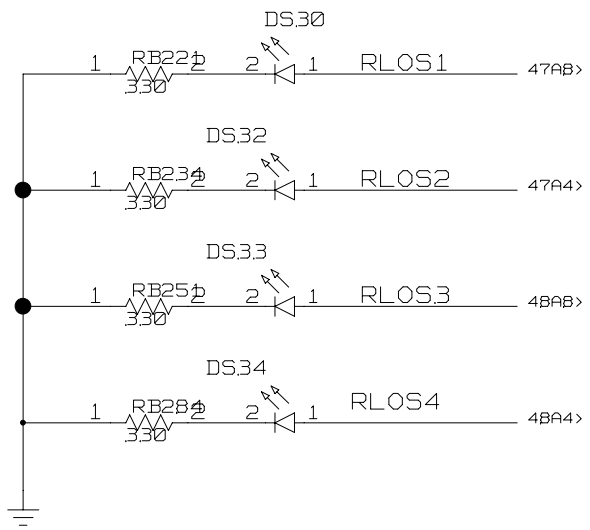
TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 5/10(BLOCK) 50/71(TOTAL)

CR-51 : @_ZTOP_LIB\._ZTOPDN_\(SCH_1):PAGE1_T11@_ZTOP_LIB\._WAN4Z44_DN\(SCH_1):PAGE1_T1@_ZTOP_LIB\._QUADTE1WAN_DN\(SCH_1):PAGE5

ALL UNMARKED BIAS RESISTORS ARE 10K



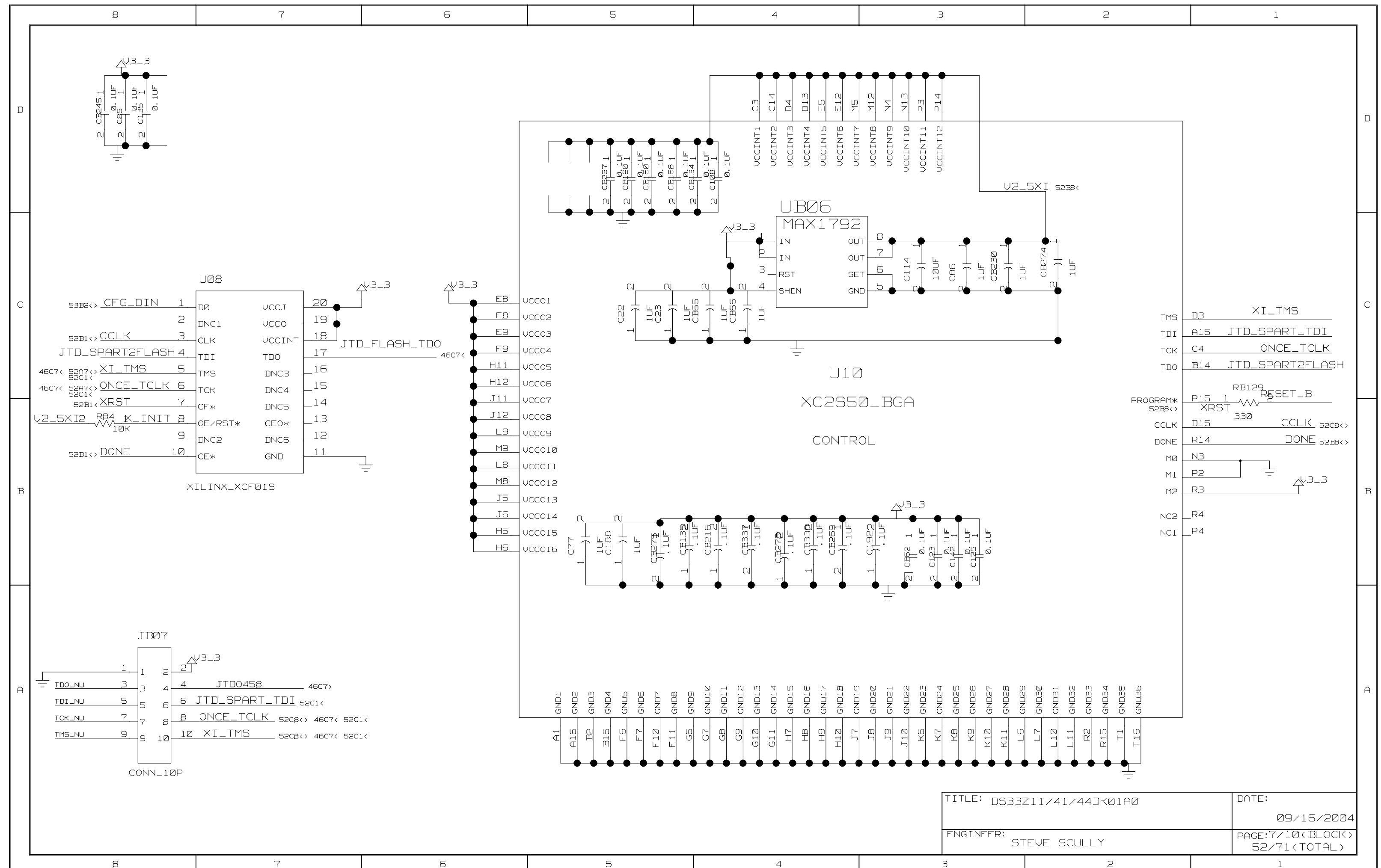




TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:6/10(BLOCK) 51/71(TOTAL)

BLOCK NAME: _quadte1wan_dn. PARENT BLOCK: _wan4z44_dn\

CR-52 : @_ZTOP_LIB\._ZTOPDN_\(SCH_1):PAGE1_T11@_ZTOP_LIB\._WAN4Z44_DN\(SCH_1):PAGE1_T1@_ZTOP_LIB\._QUADTE1WAN_DN\(SCH_1):PAGE7



TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 7/10 (BLOCK) 52/71 (TOTAL)

BLOCK NAME: _quadte1wan_dn, PARENT BLOCK: _wan4z44_dn\

47B8< RSYSCLK1
47B4< RSYSCLK2
4BB8< RSYSCLK3
4BB4< RSYSCLK4
RSYSCLK

47B6< TSYSCLK1
47B2< TSYSCLK2
4BB5< TSYSCLK3
4BB1< TSYSCLK4
TSYSCLK

BANK 1

	C9	GCK2	
	B13	IO1_1\CS*	
	C13	IO2_1\WRITE*	
	A14	IO3_1	
	C11	IO4_1\VREF	
	E11	IO5_1	
	B11	IO6_1	RSYNC1 47B8<>
	A11	IO7_1	TSYNC1 47B6<
	C10	IO8_1	
	B9	IO9_1\VREF	
	D9	IO10_1	RSYNC2 47B4<>
	A8	IO11_1	TSYNC2 47B2<
	C12	IO12_1	RSYNC3 4BB8<>
	D12	IO13_1	TSYNC3 4BB5<
	B12	IO14_1	RSYNC4 4BB4<>
	A13	IO15_1	TSYNC4 4BB1<
	D11	IO16_1	
	A12	IO17_1	TSYNC1 47B6<>
	B10	IO18_1	TSYNC2 47B2<>
	D10	IO19_1	TSYNC3 4BB5<>
	A10	IO20_1	TSYNC4 4BB1<>
	E10	IO21_1	
	A9	IO22_1	

47B6> BPCLK1

B8	GCK3	
A7	IO1_0	
B7	IO2_0\VREF	
C7	IO3_0	
B6	IO4_0	
A5	IO5_0	46D7< MCLK2FPGA
C6	IO6_0	
B4	IO7_0\VREF	
A3	IO8_0	47B8< RGAPCLK1
B3	IO9_0	47B4< RGAPCLK2
D8	IO10_0	4BB8< RGAPCLK3
A6	IO11_0	4BB4< RGAPCLK4
C8	IO12_0	47C8> RCLK1
D7	IO13_0	47C4> RCLK2
E7	IO14_0	4BC8> RCLK3
B5	IO15_0	4BC4> RCLK4
D6	IO16_0	53C2< 47B8> RSER1
A4	IO17_0	53C2< 47B4> RSER2
E6	IO18_0	53C2< 4BB8> RSER3
D5	IO19_0	53C2< 4BB4> RSER4
C5	IO20_0	

U10

XC2S50_BGA

BANK 0

BANK 2

IO2_1\IRDY	H16	
IO2_2\VREF	H15	
IO3_2\D3	G16	
IO4_2	H13	
IO5_2	G13	
IO6_2\D2	F15	
IO7_2\D1	E16	SPARE_TP1 TP32
IO8_2	F14	SPARE_TP2 TP30
IO9_2	D16	
IO10_2\VREF	F13	
IO11_2	E13	TSER1 47B5<
IO12_2\<DIN,D0>	D14	CFG_DIN 52C8<>
IO13_2\<DOUT,BUSY>	C15	
IO14_2	H14	TSER2 47B1<
IO15_2	J13	TSER3 4BB5<
IO16_2	G14	TSER4 4BB1<
IO17_2	G15	TCLK1 47C5<
IO18_2	G12	TCLK2 47C1<
IO19_2	F16	TCLK3 4BC5<
IO20_2	F12	TCLK4 4BC1<
IO21_2	E15	TGAPCLK1 47B5<>
IO22_2	E14	TGAPCLK2 47B1<>
IO23_2	C16	TGAPCLK3 4BB5<>
IO24_2	B16	TGAPCLK4 4BB1<>

BANK 3

N15	IO1_3\INIT*	
N14	IO2_3\D7	
M13	IO3_3	
L14	IO4_3\VREF	
P16	IO5_3	
L13	IO6_3	
N16	IO7_3\D6	
M16	IO8_3\D5	
K14	IO9_3	
K16	IO10_3\VREF	
J16	IO11_3\D4	
K15	IO12_3	
J15	IO13_3\TRDY	
T15	IO14_3	
R16	IO15_3	
M14	IO16_3	
M15	IO17_3	
L12	IO18_3	
L16	IO19_3	
K13	IO20_3	
L15	IO21_3	
K12	IO22_3	
J14	IO23_3	

X_INIT
52B8<>

TSER PULLDNS USED IN IBO MODE
(IMPLEMENTS IMUX)

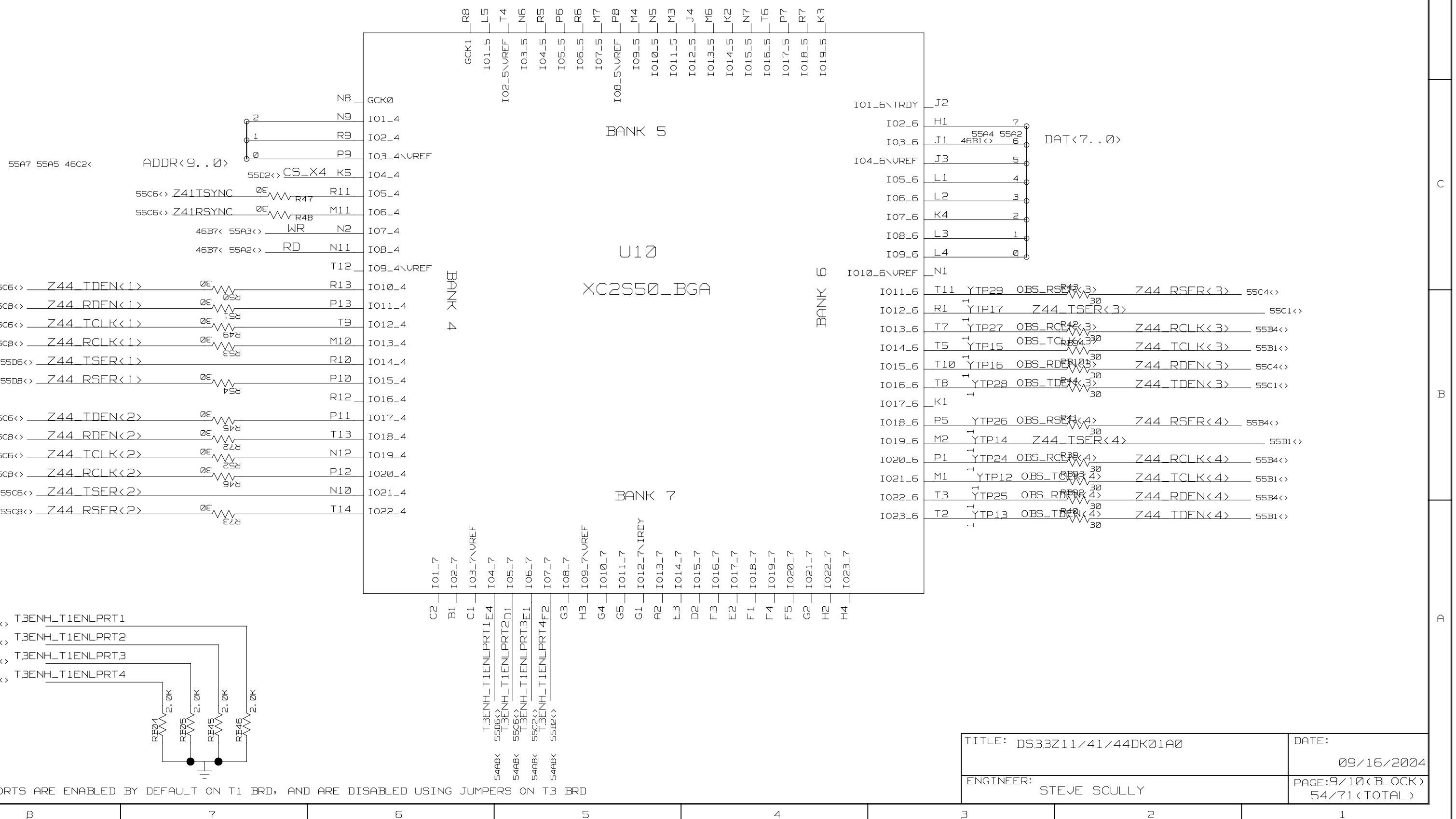
53A7<> 47B8> RSER1
53A7<> 47B4> RSER2
53A7<> 4BB8> RSER3
53A7<> 4BB4> RSER4

R88 2.0K
R113 2.0K
R104 2.0K
R94 2.0K

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:8/10(BLOCK) 53/71(TOTAL)

BLOCK NAME: _quadte1wan_dn. PARENT BLOCK: _wan4z44_dn\

CR-54 : @_ZTOP_LIB\._ZTOPDN_\(SCH_1):PAGE1_T11@_ZTOP_LIB\._WAN4Z44_DN\(SCH_1):PAGE1_T1@_ZTOP_LIB\._QUADTE1WAN_DN\(SCH_1):PAGE9



TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:9/10(BLOCK) 54/71(TOTAL)

BLOCK NAME: _quadte1wan_dn. PARENT BLOCK: _wan4z44_dn\

CR-55 : @_ZTOP_LIB\._ZTOPDN_\(SCH_1):PAGE1_I11@_ZTOP_LIB\._WAN4Z44_DN\(SCH_1):PAGE1_I1@_ZTOP_LIB\._QUADTE1WAN_DN\(SCH_1):PAGE10

V3_3
V3_3
GND

RECEPTACLE
P2 CONNECTOR (RECEPTICAL)

J12

VDD

I28
INT3 — WAN_INT 46A4<> 46C7>

INT5
55D6<> INT2
RESET_B 46A2<> 52B1<
INT2 55D7<>

54B8< Z44_RSER<1> — T3ENH_T1ENLPRT1 54A6<> 54AB<
Z44_TSER<1> 54B8<>
54B8< Z44_RDEN<1> — SIG_RETURN 55A1> 55B2<> 55C6<>
Z44_TDEN<1> 54B8<
54B8< Z44_RCLK<1> — Z44_TCLK<1> 54B8<
Z41RSYNC 54C7<
Z41TSYNC 54C7<
T3ENH_T1ENLPRT2 54A5<> 54AB<
54AB< Z44_RSER<2> — SIG_RETURN 55A1> 55B2<> 55C6<>
Z44_TSER<2> 54B8<>
54B8< Z44_RDEN<2> — Z44_TDEN<2> 54B8<
54B8< Z44_RCLK<2> — Z44_TCLK<2> 54B8<

TDO_NU 52AB<>
TCK_NU 52AB<>
52AB<> TDI_NU
52AB<> TMS_NU

ADDR<9..0> — ADDR<9..0> 46C2< 54C7 55A7
55A2 54C3 46B1<>

55A5
46C2< 54C7

OSC2_NU
OSC4_NU
OSC3_NU

P1 CONNECTOR (RECEPTICAL)
RECEPTACLE

J09

ALE
CS_X4 54C7<>
CS_X5

54B1< Z44_RSER<3> — T3ENH_T1ENLPRT3 54A5<> 54AB<
Z44_TSER<3> 54B1<>
54B1< Z44_RDEN<3> — Z44_TDEN<3> 54B1<
54B1< Z44_RCLK<3> — Z44_TCLK<3> 54B1<
T3ENH_T1ENLPRT4 54A5<> 54AB<
54B1< Z44_RSER<4> — Z44_TSER<4> 54B1<>
54B1< Z44_RDEN<4> — Z44_TDEN<4> 54A1<
54B1< Z44_RCLK<4> — SIG_RETURN 55A1> 55C6<>
Z44_TCLK<4> 54B1<

DAT<7..0> — DAT<7..0>
55A4
54C3 46B1<>

46B7< CS — CS_X2
CS_X3
46B7< 54C7<> WR
RD 54C7<> 46B7<

NOTE 3184 IS ON CS3 WHILE 21455 IS ON CS2/CS4

WAN R.C. CONNECTOR TO MOTHERBOARD

I27
GND — SIG_RETURN

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 10/10 (BLOCK) 55/71 (TOTAL)

BLOCK NAME: _quadte1wan_dn. PARENT BLOCK: _wan4z44_dn\

CR-55 : @_ZTOP_LIB\._ZTOPDN_\(SCH_1):PAGE1_I11@_ZTOP_LIB\._WAN4Z44_DN\(SCH_1):PAGE1_I2@_ZTOP_LIB\._QUADTE3WAN_DN\(SCH_1):PAGE1

DS3184 WAN INTERFACE BLOCK

J39

CONN_10P

UB08

DS3184

CONTROL

DS41

ADDR<10..0>

DAT<7..0>

VALUE NOT SHOWN FOR 10K RES

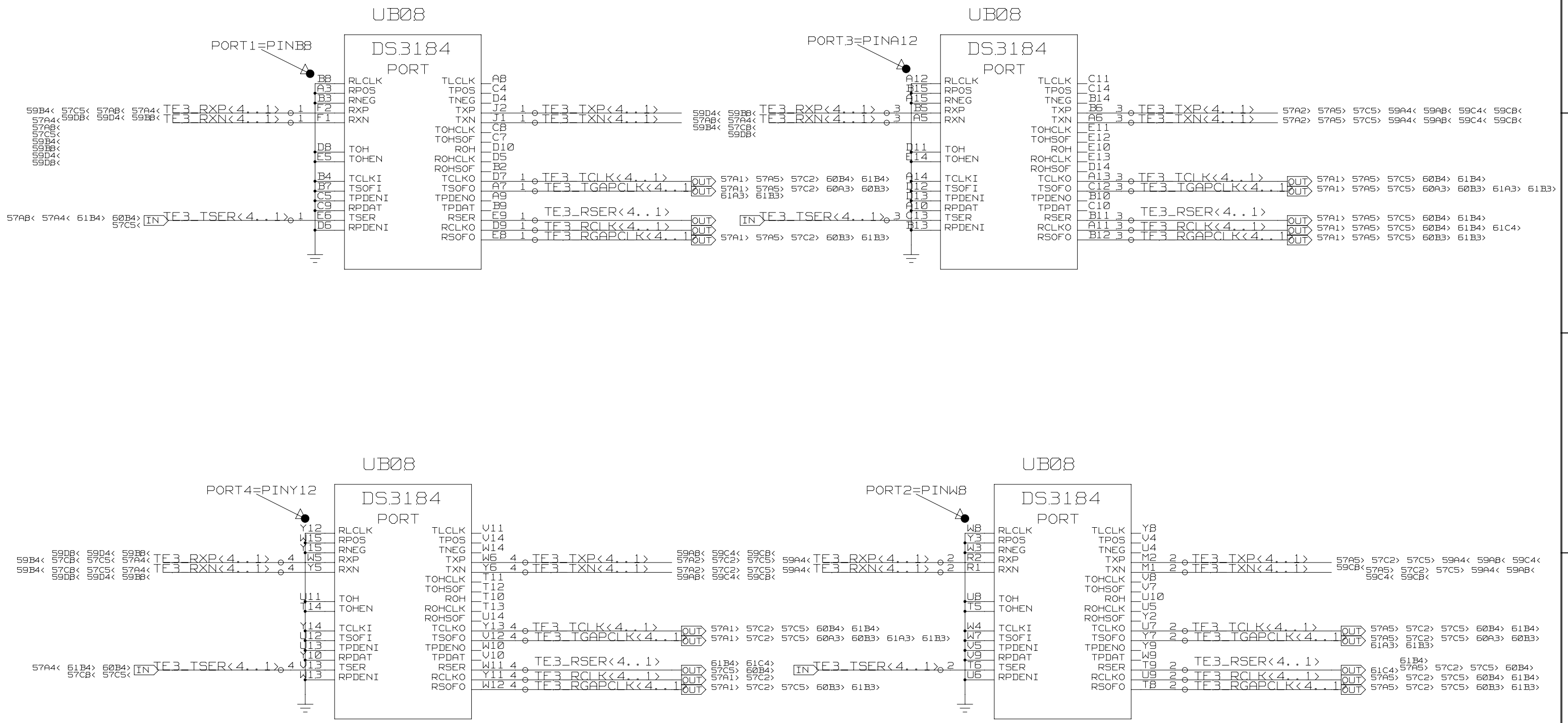
TITLE: DS3.3.3Z11/41/44DK01A0

DATE: 09/16/2004

ENGINEER: STEVE SCULLY

PAGE: 1/8 (BLOCK) 56/71 (TOTAL)

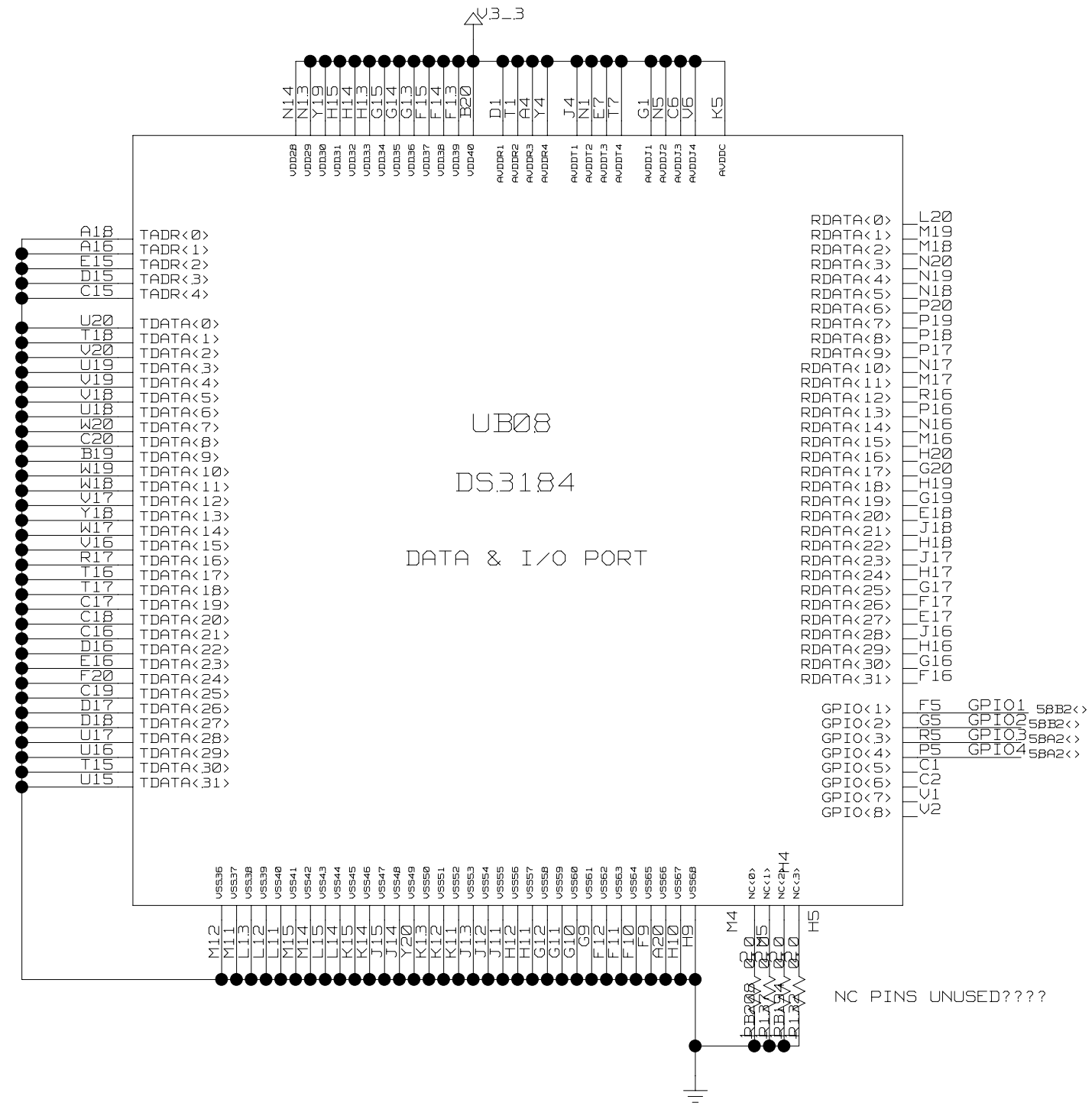
CR-57 : @_ZTOP_LIB\._ZTOPDN_\(SCH_1):PAGE1_I11@_ZTOP_LIB\._WAN4Z44_DN\(SCH_1):PAGE1_I2@_ZTOP_LIB\._QUADTE3WAN_DN\(SCH_1):PAGE2



TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 2/8 (BLOCK) 57/71 (TOTAL)

BLOCK NAME: _quadte3wan_dn. PARENT BLOCK: _wan4z44_dn\

CR-5B : @_ZTOP_LIB\._ZTOPDN_\(SCH_1):PAGE1_I11@_ZTOP_LIB\._WAN4Z44_DN\(SCH_1):PAGE1_I2@_ZTOP_LIB\._QUADTE3WAN_DN\(SCH_1):PAGE3

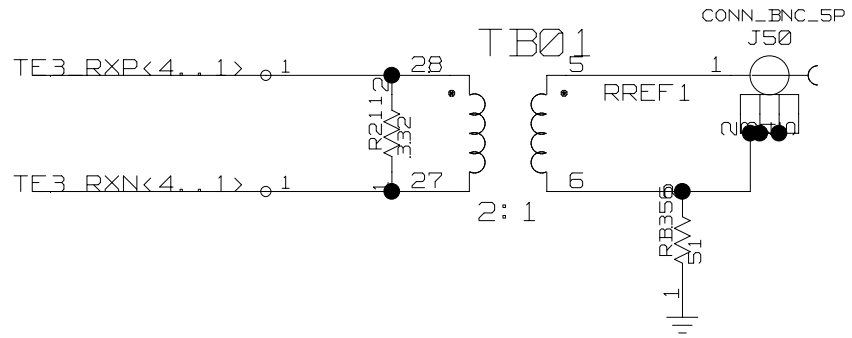


TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 3/8 (BLOCK) 58/71 (TOTAL)

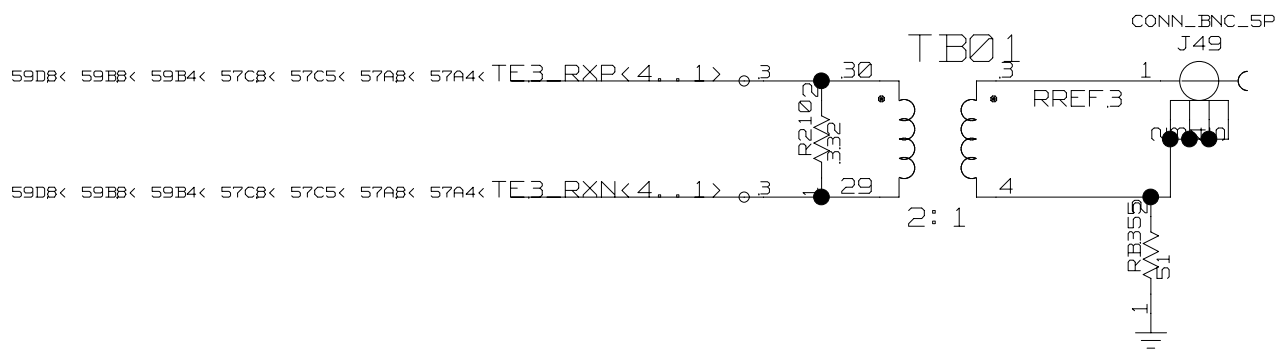
BLOCK NAME: _quadte3wan_dn, PARENT BLOCK: _wan4z44_dn\

CR-59 : @_ZTOP_LIB\._ZTOPDN_\(SCH_1):PAGE1_I11@_ZTOP_LIB\._WAN4Z44_DN\(SCH_1):PAGE1_I2@_ZTOP_LIB\._QUADTE3WAN_DN\(SCH_1):PAGE4

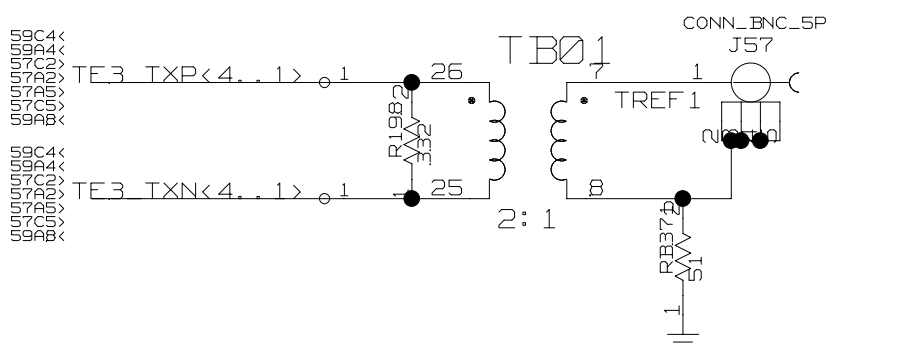
75 OHM VERT



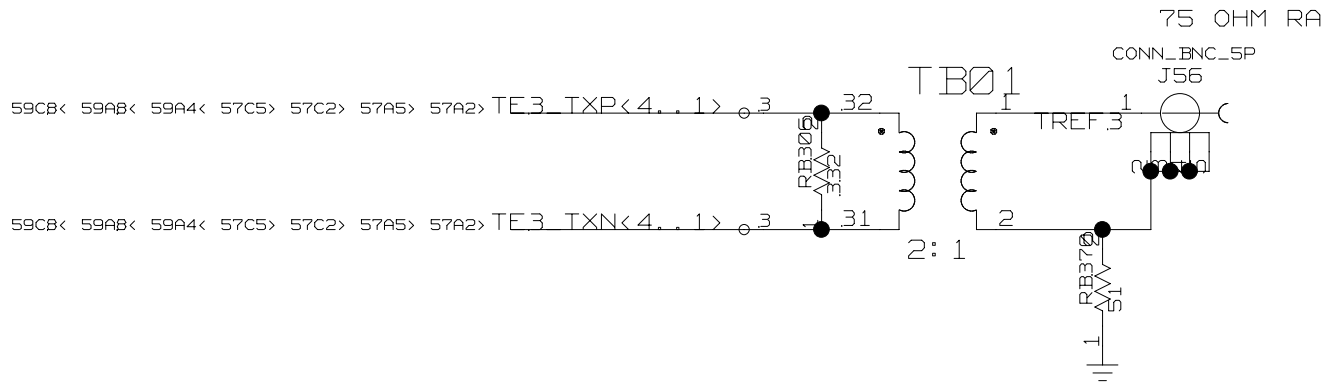
75 OHM VERT



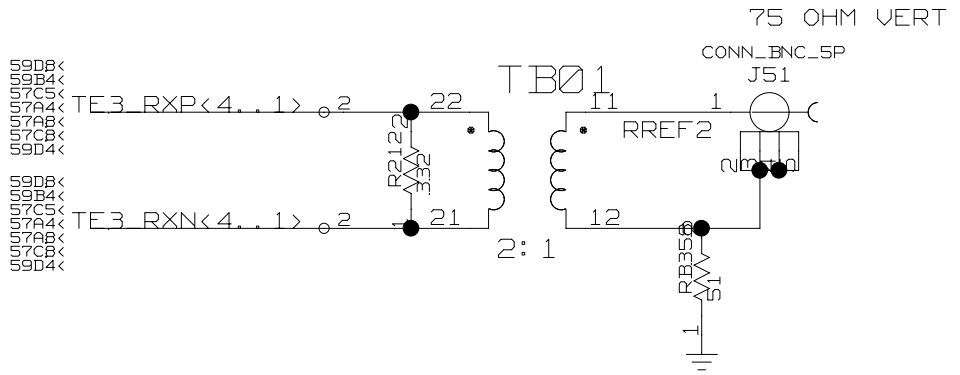
75 OHM RA



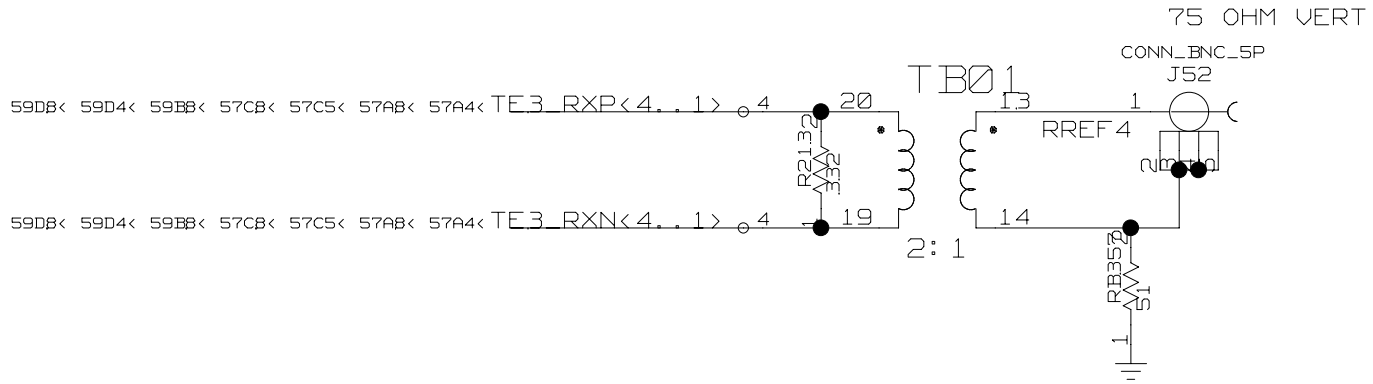
75 OHM RA



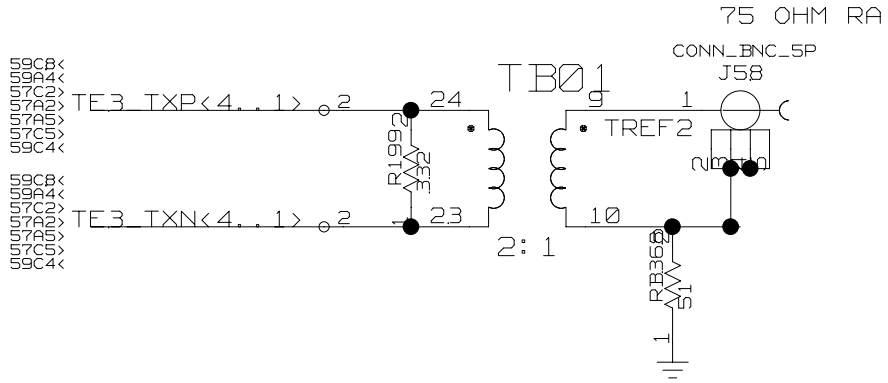
75 OHM VERT



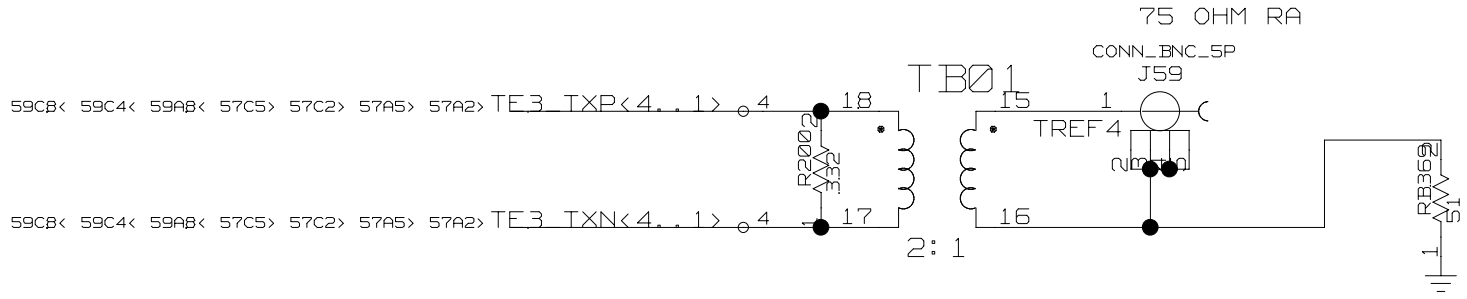
75 OHM VERT



75 OHM RA



75 OHM RA



TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:4/8(BLOCK) 59/71(TOTAL)

BLOCK NAME: _quadte3wan_dn. PARENT BLOCK: _wan4z44_dn\

CR-60 : @_ZTOP_LIB\,_ZTOPDN_\(SCH_1):PAGE1_I11@_ZTOP_LIB\,_WAN4Z44_DN\(SCH_1):PAGE1_I12@_ZTOP_LIB\,_QUADTE3WAN_DN\(SCH_1):PAGE5

Z44 CONNECTIONS

XILINX_XC9572XL

XILINX_CPLD

UB04

XILINX_CPLD

UB03

XILINX_XC9572XL

44.736MHZ_5.0V

Y08

OSC

PORTS ARE ENABLED BY DEFAULT ON T1 BRD
AND ARE DISABLED USING JUMPERS ON T3 BRD

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE:5/8(BLOCK) 60/71(TOTAL)

BLOCK NAME: _quadte3wan_dn, PARENT BLOCK: _wan4z44_dn\

CR-61 : @_ZTOP_LIB\._ZTOPDN_\(SCH_1):PAGE1_I11@_ZTOP_LIB\._WAN4Z44_DN\(SCH_1):PAGE1_I12@_ZTOP_LIB\._QUADTE3WAN_DN\(SCH_1):PAGE6

Z44 CONNECTIONS

XILINX_XC9572XL

XILINX_CPLD

UB03

XILINX_CPLD

UB04

XILINX_XC9572XL

I79 TINYTESTPOINT

OSC_A

JMP_3M

T3ENH_T1ENLPRT3

T3ENH_T1ENLPRT4

JP18

JP16

LOOPBACK_CTRL

SPARE_TP3

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 6/8 (BLOCK) 61/71 (TOTAL)

BLOCK NAME: _quadte3wan_dn. PARENT BLOCK: _wan4z44_dn\

CR-62 : @_ZTOP_LIB\._ZTOPDN_\(SCH_1):PAGE1_I11@_ZTOP_LIB\._WAN4Z44_DN\(SCH_1):PAGE1_I2@_ZTOP_LIB\._QUADTE3WAN_DN\(SCH_1):PAGE7

V3_3

V3_3

GND

RECEPTACLE
P2 CONNECTOR (RECEPTICAL)

J10

VDD

GND
6,3D7<> INT5
6,3D7<> 6,3D6<> 62D6<> INT2
GND
V3_3
60D6< 6,3D8<> Z44_RSER<1>
6,3B3<> 6,3A1> 62C6<> 62B3<> 62A1> SIG_RETURN
6,3C8<> 6,3C6<>
GND
60D5< 6,3C8<> Z44_RDEN<1>
GND
60D5< 6,3C8<> Z44_RCLK<1>
GND
V3_3
GND
60D7< 6,3C8<> Z44_RSER<2>
GND
60D6< 6,3C8<> Z44_RDEN<2>
GND
60D6< 6,3C8<> Z44_RCLK<2>
V3_3
GND
GND
GND
V3_3
GND
GND
GND
GND
V3_3
GND
62B3<> FPGAGCLK1_NU
GND
6,3B7<> 56D6<> TDI_NU
6,3B7<> 56D6<> TMS_NU
V3_3
0
2
GND
4
62A6 6,3A6 6,3A7
56D4< GND
7
9
GND
V3_3
6,3A7<> OSC2_NU
6,3A7<> OSC4_NU

I36
6,3D6<> INT3
INT4
6,3D6<>
GND
INT2 6,2D7<> 6,3D6<> 6,3D7<>
RESET_B 6,3D6<> 56B8<
GND
T3ENH_T1ENLPRT1 60AB<> 60CB<> 6,3D6<>
Z44_TSER<1> 60D6<> 6,3D6<>
GND
Z44_TDEN<1> 6,3C6<> 60D5<
Z44_TCLK<1> 6,3C6<> 60D5<
GND
GND
T3ENH_T1ENLPRT2 60AB<> 60CB<> 6,3C6<>
GND
SIG_RETURN 62A1> 62B3<> 62CB<> 6,3A1> 6,3B3<> 6,3C6<> 6,3CB<>
Z44_TSER<2> 60D7<> 6,3C6<>
Z44_TDEN<2> 6,3C6<> 60D6<
GND
Z44_TCLK<2> 6,3C6<> 60D6<
GND
GND
GND
GND
GND
GND
GND
TDO_NU 56D6<> 6,3B6<>
TCK_NU 56D7<> 6,3B6<>
GND
GND
1
3
5
ADDR<10..0>
6
8
GND
10
GND
ADDR<10..0> 6,3A5 6,3A3 62A3 56C3<>
GND
OSC3_NU 6,3A6<>
GND

T3_INT 56A6<> 56B8> 6,3D5>

RECEPTACLE
P1 CONNECTOR (RECEPTICAL)

J07

GND
6,3D4<> CS_X5
GND
V3_3
GND
GND
V3_3
GND
GND
GND
GND
V3_3
GND
GND
GND
GND
V3_3
GND
GND
GND
GND
V3_3
GND
6,3A4<> OSC1_NU
GND
2
4
GND
DAT<7..0>
6
6,3A4<> CS_X2
V3_3
6,3A5< 56B7< 6,3A4<> CS CS_X3
56B8< 6,3A4<> WR
GND

ALE 6,3D3<>
CS_X4 6,3D3<>
GND
GND
GND
GND
GND
GND
GND
GND
T3ENH_T1ENLPRT3 61AB<> 61CB<> 6,3C2<>
Z44_TSER<3> 61D6<> 6,3C2<>
GND
61D6< 6,3C5<> Z44_RSER<3>
Z44_TDEN<3> 6,3C2<> 61D5<
GND
61D5< 6,3C5<> Z44_RDEN<3>
GND
61D5< 6,3C5<> Z44_RCLK<3>
Z44_TCLK<3> 6,3C2<> 61D5<
GND
GND
GND
T3ENH_T1ENLPRT4 61AB<> 61CB<> 6,3B2<>
61D7< 6,3B5<> Z44_RSER<4>
Z44_TSER<4> 61D7<> 6,3B2<>
GND
61D6< 6,3B5<> Z44_RDEN<4>
Z44_TDEN<4> 6,3B2<> 61D6<
GND
SIG_RETURN 62A1> 62C6<> 62CB<> 6,3A1> 6,3B3<> 6,3C6<> 6,3CB<>
61D6< 6,3B5<> Z44_RCLK<4>
Z44_TCLK<4> 6,3B2<> 61D6<
GND
FPGAGCLK1_NU 62B7<>
GND
GND
GND
GND
0
1
3
5
DAT<7..0>
7
GND
6,3A3<> RW RD 6,3A3> 56B8<
GND

WAN R.C. CONNECTOR TO MOTHERBOARD

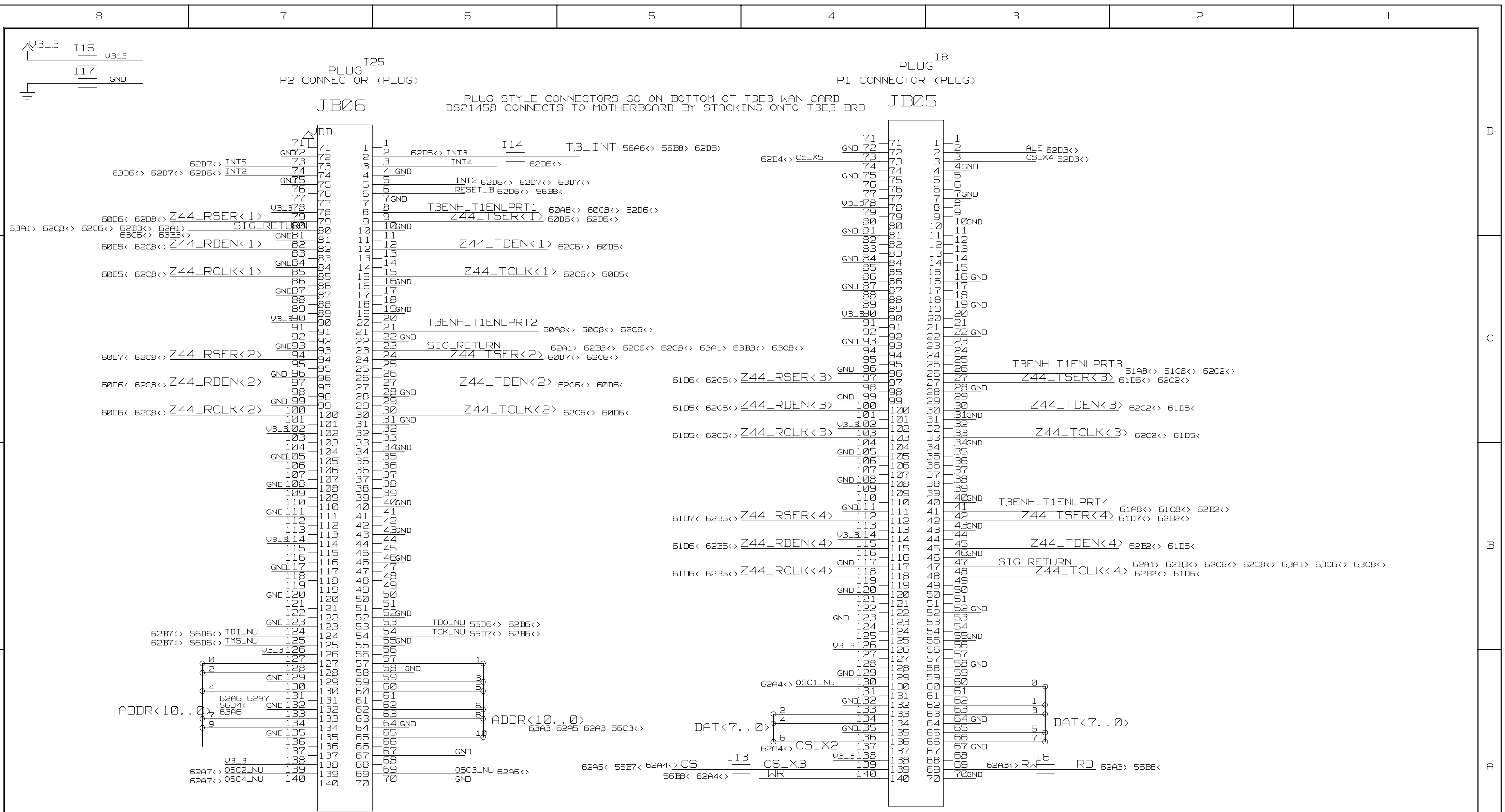
NOTE 3184 IS ON CS3 WHILE 21455 IS ON CS2/CS4

I35
GND SIG_RETURN 62B3<> 62C6<> 62CB<> 6,3A1>
6,3B3<> 6,3C6<> 6,3CB<>

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 7/8 (BLOCK) 62/71 (TOTAL)

BLOCK NAME: _quadte3wan_dn. PARENT BLOCK: _wan4z44_dn\

CR-6.3 : @_ZTOP_LIB\._ZTOPDN_\(SCH_1):PAGE1_I11@_ZTOP_LIB\._WAN4Z44_DN\(SCH_1):PAGE1_I2@_ZTOP_LIB\._QUADTE3WAN_DN\(SCH_1):PAGE8



WAN R.C. CONNECTOR TO MOTHERBOARD

NOTE 3184 IS ON CS3 WHILE 21455 IS ON CS2/CS4

TITLE: DS33Z11/41/44DK01A0	DATE: 09/16/2004
ENGINEER: STEVE SCULLY	PAGE: 8/8 (BLOCK) 63/71 (TOTAL)

BLOCK NAME: _quadte3wan_dn. PARENT BLOCK: _wan4z44_dn\